



US006300786B1

(12) **United States Patent**
Doherty et al.

(10) **Patent No.:** US 6,300,786 B1
(45) **Date of Patent:** Oct. 9, 2001

(54) **WAFER TEST METHOD WITH PROBE CARD HAVING ON-BOARD MULTIPLEX CIRCUITRY FOR EXPANDING TESTER RESOURCES**

(75) Inventors: **C. Patrick Doherty; Jorge L. deVarona; Salman Akram**, all of Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

5,055,780	10/1991	Takagi et al. .	
5,070,297	12/1991	Kwon et al. .	
5,103,557	4/1992	Leedy .	
5,124,639	6/1992	Carlin et al. .	
5,172,050	12/1992	Swapp .	
5,177,439	1/1993	Liu et al. .	
5,180,977	1/1993	Huff .	
5,225,037	7/1993	Elder et al. .	
5,264,787	11/1993	Woith et al. .	
5,323,107	6/1994	D'Souza .	
5,326,428 *	7/1994	Farnworth et al.	324/724
5,329,423	7/1994	Scholz .	
5,419,809 *	5/1995	Akram et al.	324/724
5,430,614	7/1995	DiFrancesco .	

(List continued on next page.)

(21) Appl. No.: **09/420,256**

(22) Filed: **Oct. 18, 1999**

OTHER PUBLICATIONS

Related U.S. Application Data

U.S. application No. 09/075,691, Doherty et al.

(62) Division of application No. 09/075,691, filed on May 11, 1998.

(51) **Int. Cl.**⁷ **G01R 31/26; G01R 31/02; H05K 3/36; H01R 43/16; H01R 43/04**

(52) **U.S. Cl.** **324/765; 324/754; 324/537; 324/158.1; 438/6; 29/830; 29/874; 29/882; 29/829**

(58) **Field of Search** **324/765, 754, 324/537, 158.1; 438/6; 29/830, 874, 882, 829**

Primary Examiner—Glenn W. Brown

Assistant Examiner—Wasseem H. Hamdan

(74) *Attorney, Agent, or Firm*—Stephen A. Gratton

(57) ABSTRACT

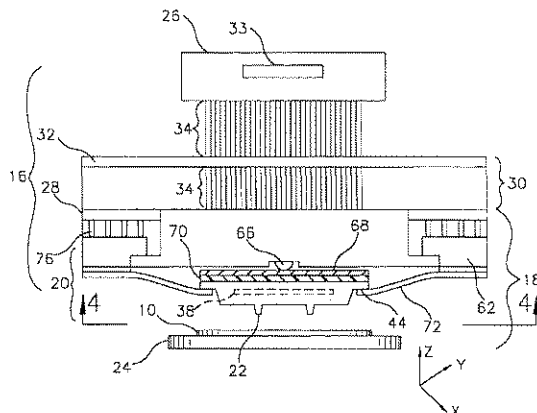
A probe card, a test method and a test system for testing semiconductor wafers are provided. The test system includes the probe card, a tester for generating test signals, and a wafer prober for placing the wafers and probe card in physical contact. The probe card includes contacts for electrically engaging die contacts on the wafer. The probe card also includes an on board multiplex circuit adapted to fan out and selectively transmit test signals from the tester to the probe card contacts. The multiplex circuit expands tester resources by allowing test signals to be written to multiple dice in parallel. Reading of the dice can be performed in groups up to the limit of the tester resources. In addition to expanding tester resources, the multiplex circuit maintains the individuality of each die, and permits defective dice to be electrically disconnected.

(56) References Cited

U.S. PATENT DOCUMENTS

3,806,801	4/1974	Bove .
4,027,935	6/1977	Byrnes et al. .
4,585,991	4/1986	Reid et al. .
4,891,585	1/1990	Janko et al. .
4,906,920	3/1990	Huff et al. .
4,918,383	4/1990	Huff et al. .
4,954,458	9/1990	Reid .
5,042,148	8/1991	Tada et al. .
5,053,700	10/1991	Parrish .

16 Claims, 7 Drawing Sheets



US 6,300,786 B1

Page 2

U.S. PATENT DOCUMENTS

5,475,317	12/1995	Smith .	5,915,977	6/1999	Hembree et al. .
5,477,160	12/1995	Love .	5,952,840	9/1999	Farnworth et al. .
5,483,741	1/1996	Akram et al. .	5,962,921	10/1999	Farnworth et al. .
5,625,298	4/1997	Hirano et al. .	6,016,060	1/2000	Akram et al. .
5,678,301	10/1997	Gochmour et al. .	6,040,702	3/2000	Hembree et al. .
5,686,317	11/1997	Akram et al. .	6,060,891	5/2000	Hembree et al. .
5,736,850	4/1998	Legal .	6,072,321	6/2000	Akram et al. .
5,789,271	8/1998	Akram .	6,078,186	6/2000	Hembree et al. .
5,834,945	11/1998	Akram et al. .	6,091,252	7/2000	Akram et al. .
5,869,974	2/1999	Akram et al. .	6,107,109	8/2000	Akram et al. .
5,894,161	4/1999	Akram et al. .	6,127,736	10/2000	Akram .

* cited by examiner

U.S. Patent

Oct. 9, 2001

Sheet 1 of 7

US 6,300,786 B1

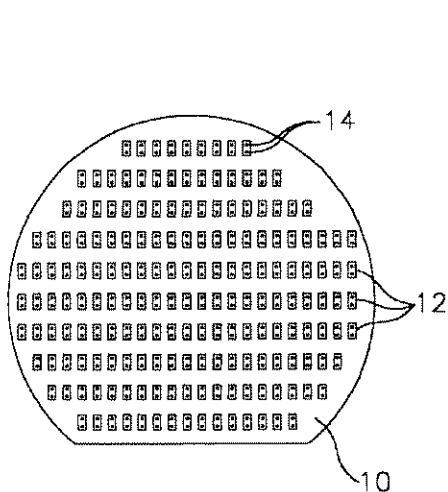


FIGURE 1
(PRIOR ART)

Vcc	1□	□28	Vss
DQ1	2□	□27	DQ8
DQ2	3□	□26	DQ7
DQ3	4□	□25	DQ6
DQ4	5□	□24	DQ5
NC	6□	□23	CAS
WE	7□	□22	OE
RAS	8□	□21	NC
A9	9□	□20	A8
A0	10□	□19	A7
A1	11□	□18	A6
A2	12□	□17	A5
A3	13□	□16	A4
Vcc	14□	□15	Vss

FIGURE 2
(PRIOR ART)

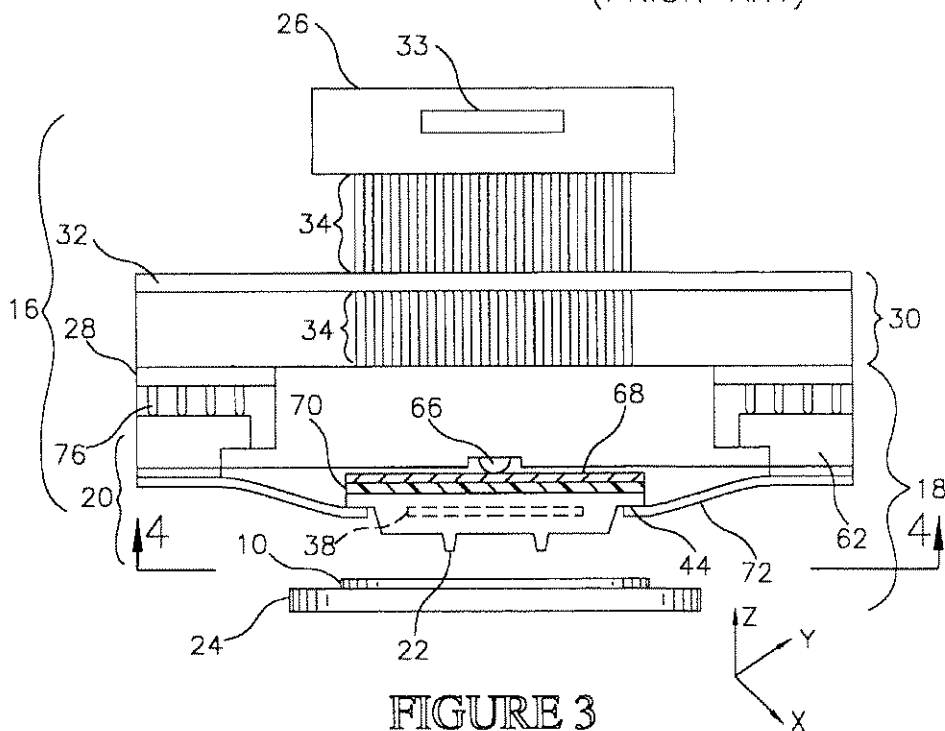


FIGURE 3

U.S. Patent

Oct. 9, 2001

Sheet 2 of 7

US 6,300,786 B1

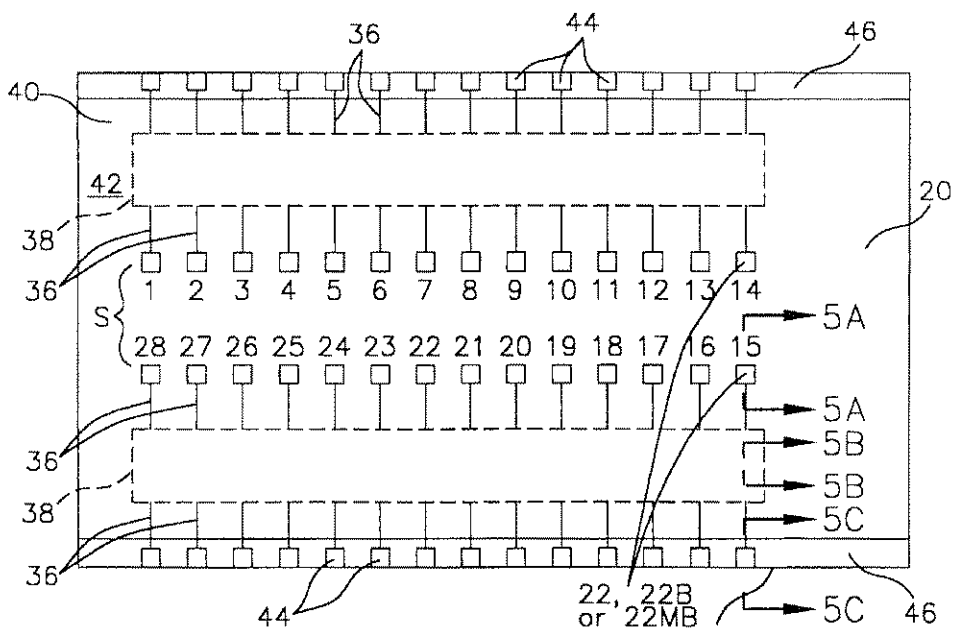


FIGURE 4

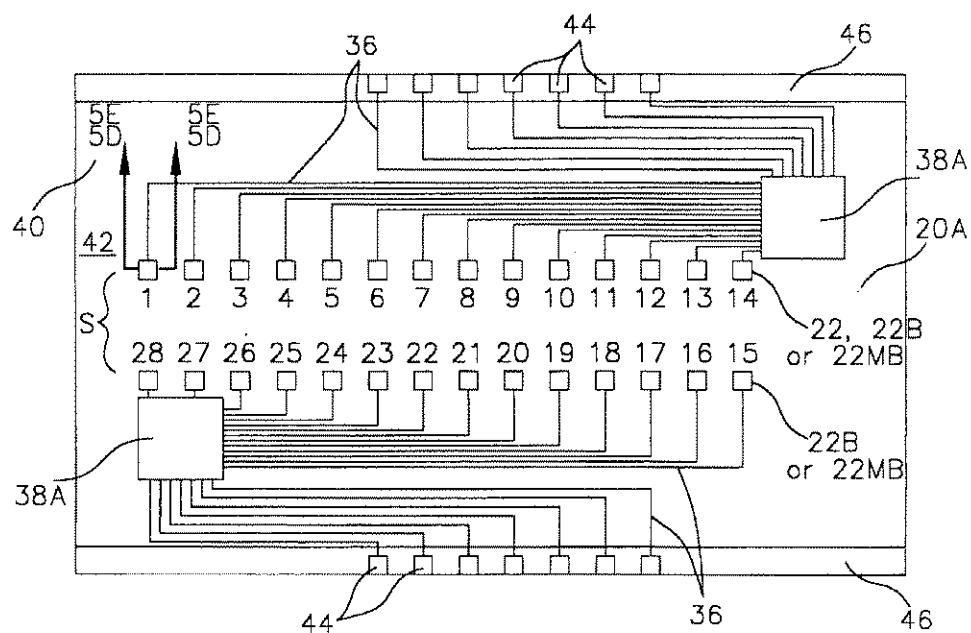


FIGURE 4A

U.S. Patent

Oct. 9, 2001

Sheet 3 of 7

US 6,300,786 B1

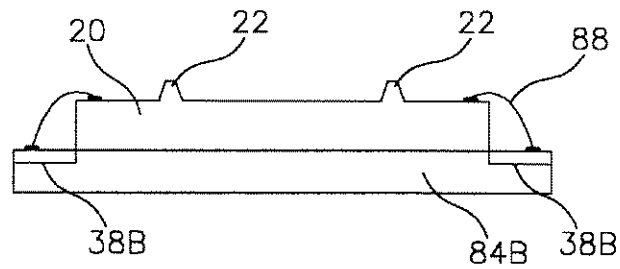


FIGURE 4B

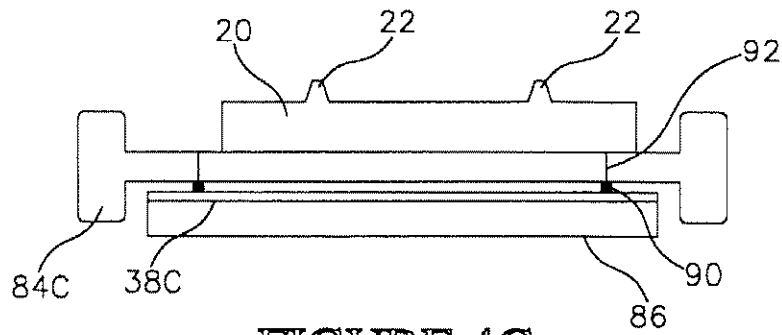


FIGURE 4C

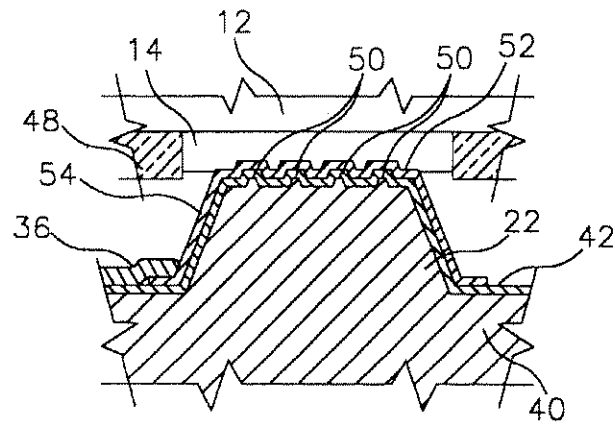


FIGURE 5A

U.S. Patent

Oct. 9, 2001

Sheet 4 of 7

US 6,300,786 B1

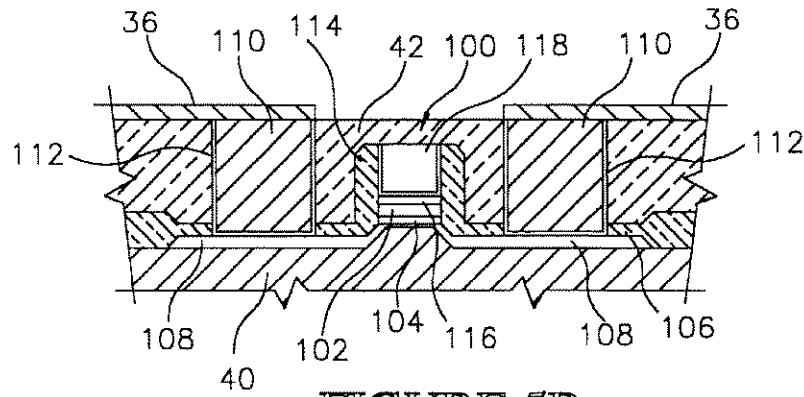


FIGURE 5B

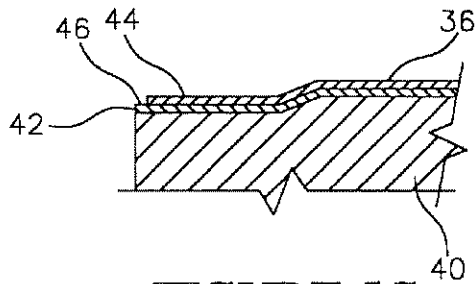


FIGURE 5C

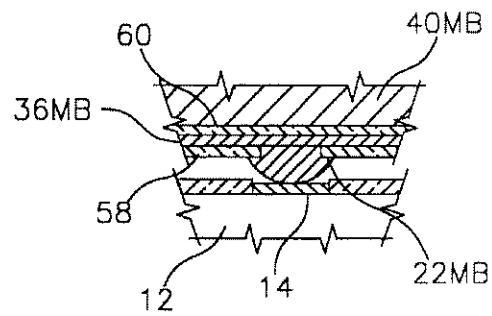


FIGURE 5D

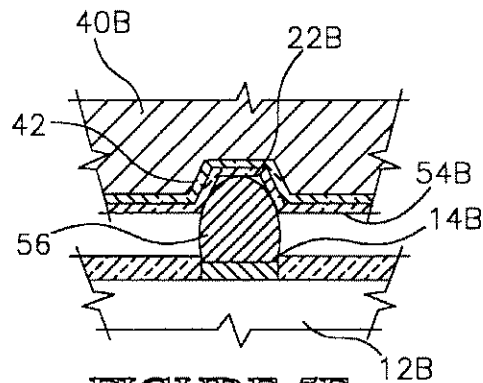


FIGURE 5E

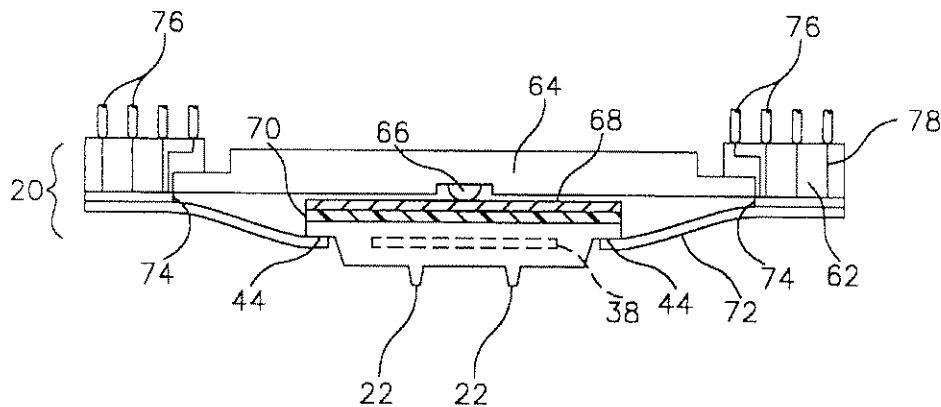


FIGURE 6

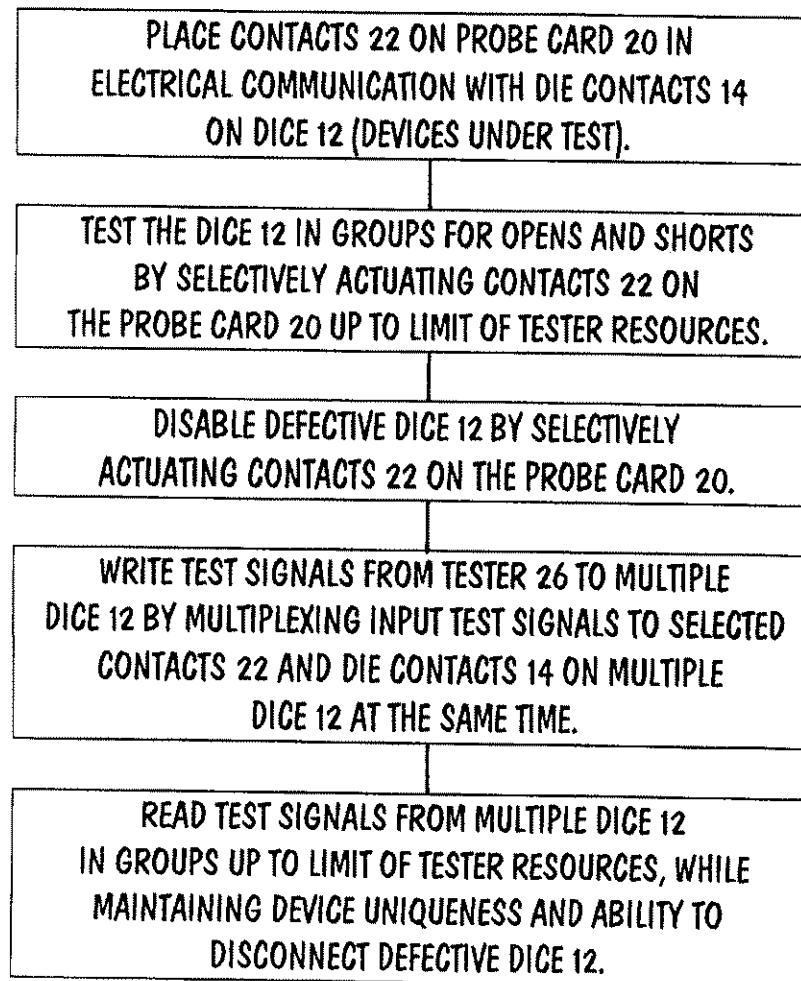


FIGURE 7

U.S. Patent

Oct. 9, 2001

Sheet 6 of 7

US 6,300,786 B1

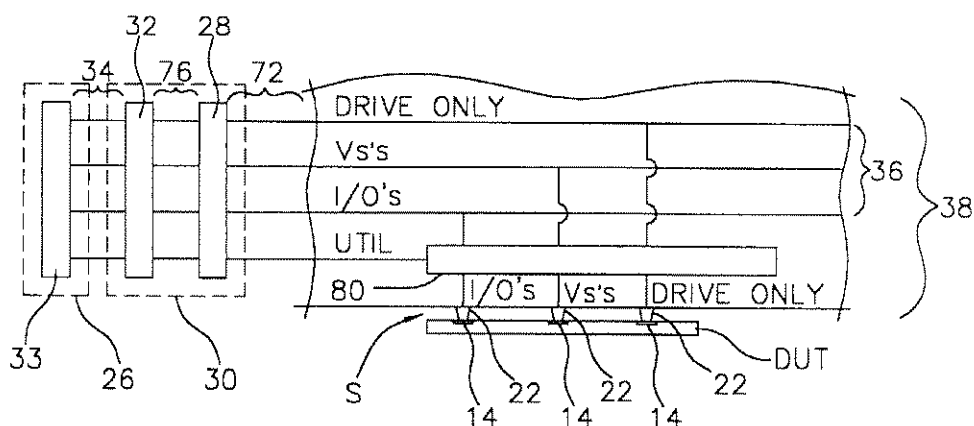


FIGURE 8A

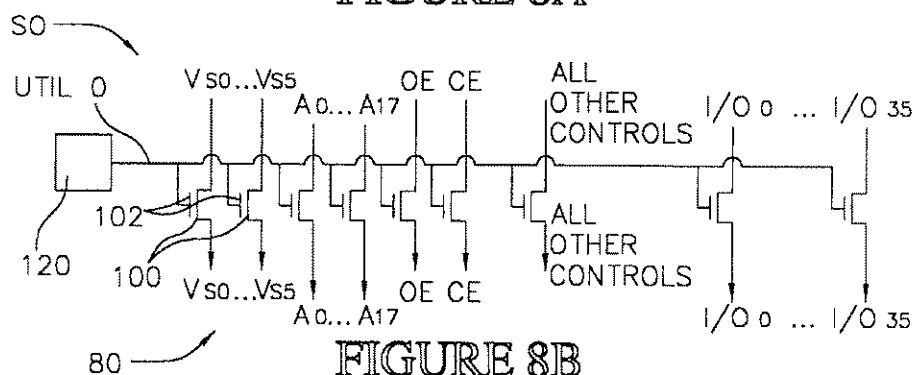


FIGURE 8B

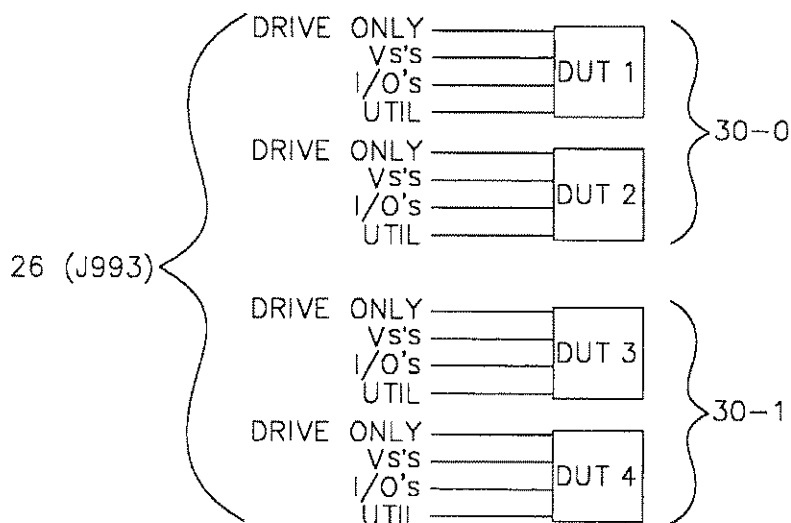


FIGURE 8C
(PRIOR ART)

U.S. Patent

Oct. 9, 2001

Sheet 7 of 7

US 6,300,786 B1

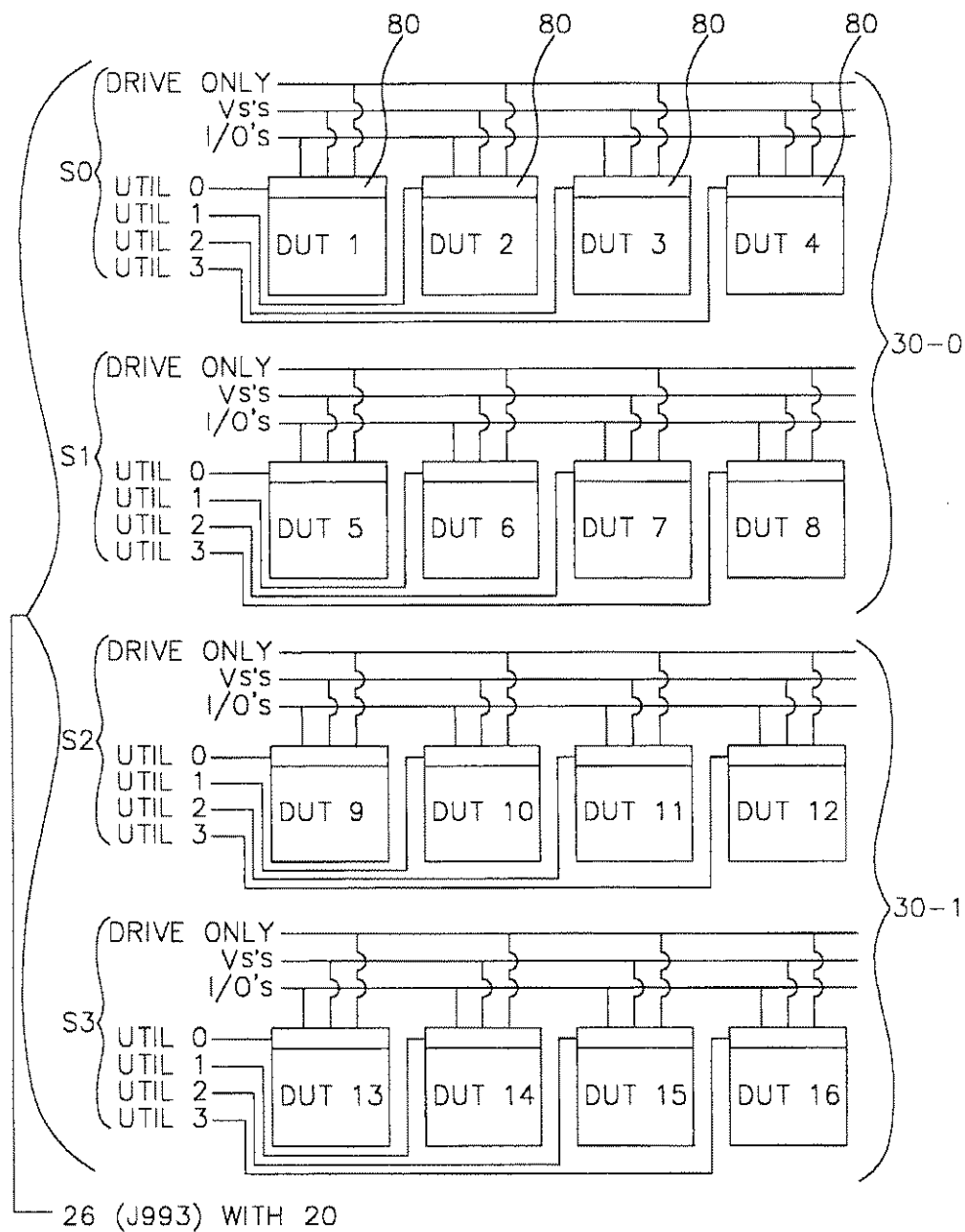


FIGURE 8D

US 6,300,786 B1

1

WAFER TEST METHOD WITH PROBE CARD HAVING ON-BOARD MULTIPLEX CIRCUITRY FOR EXPANDING TESTER RESOURCES

This application is a division of Ser. No. 09/075,691 filed May 11, 1998.

FIELD OF THE INVENTION

This invention relates generally to semiconductor manufacture and specifically to a probe card for testing semiconductor wafers. This invention also relates to test systems and test methods employing the probe card.

BACKGROUND OF THE INVENTION

Semiconductor wafers are tested prior to singulation into individual die, to assess the electrical characteristics of the integrated circuits contained on each die. A typical wafer-level test system includes a wafer prober for handling and positioning the wafers, a tester for generating test signals, a probe card for making temporary electrical connections with the wafer, and a prober interface board to route signals from the tester pin electronics to the probe card.

The test signals can include specific combinations of voltages and currents transmitted through the pin electronics channels of the tester to the probe interface board, to the probe card, and then to one or more devices under test on the wafer. During the test procedure response signals such as voltage, current and frequency can be analyzed and compared by the tester to required values. The integrated circuits that do not meet specification can be marked or mapped in software. Following testing, defective circuits can be repaired by actuating fuses to inactivate the defective circuitry and substitute redundant circuitry.

Different types of probe cards have been developed for probe testing semiconductor wafers. The most common type of probe card includes elongated needle probes configured to electrically engage die contacts, such as bond pads, or other contacts on the wafer. An exemplary probe card having needle probes is described in U.S. Pat. No. 4,563,640 to Hasegawa et al.

Although widely used, needle probe cards are difficult to maintain and unsuitable for high parallelism applications, in which multiple dice must be tested at the same time. In addition, needle probe cards are not suitable for some applications in which the dice have high count die contact requirements, such as bond pads in dense grid arrays. In particular, the long needles and variations in the needles lengths makes it difficult to apply a constant gram force to each die contact. Long needles can also generate parasitic signals at high speeds (e.g., >500 MHZ).

A similar type of probe card includes buckle beams adapted to flex upon contact with the wafer. This type of probe card is described in U.S. Pat. No. 4,027,935 to Byrnes et al. Although better for high count die contacts, and high parallelism applications, buckle beam probe cards are expensive, and difficult to maintain.

Another type of probe card, referred to as a "membrane probe card", includes a membrane formed of a thin and flexible dielectric material such as polyimide. An exemplary membrane probe card is described in U.S. Pat. No. 4,918,383 to Huff et al. With membrane probe cards, contact bumps are formed on the membrane in electrical communication with conductive traces, typically formed of copper.

One disadvantage of membrane contact bumps is that large vertical "overdrive" forces are required to penetrate

2

oxide layers and make a reliable electrical connection with the die contacts on the dice. These forces can damage the die contacts and the dice. In addition, membrane probe cards can be repeatedly stressed by the forces, causing the membrane to lose its resiliency. Use of high probe temperatures can also cause the membrane to lose resiliency.

Another disadvantage of membrane probe cards is the CTE (coefficient of thermal expansion) mismatch between the membrane probe card and wafer. In the future, with decreasing size of each die contact, higher parallelism requirements, and increased probing temperatures, maintaining electrical contact with the die contacts will be increasingly more difficult. In addition, because of relatively large differences between the CTE of membrane probe cards and silicon wafers, maintaining electrical contact between a large number of dice and a membrane probe card will be almost impossible.

Yet another limitation of conventional test systems, and a disadvantage of conventional probe cards, is that full functionality testing must be performed at the die level rather than at the wafer level. These tests require a large number of connections with the dice, and separate input/output paths between the dice and test circuitry. For functional test procedures on dice having multiple inputs and outputs, an input/output path must be provided to several die contacts at the same time. The number of dice that can be tested in parallel is always limited by the number of drive only, and input/output channels the tester provides, as well as the die contact arrangements on the dice. The number of drive only and input/output channels is fixed for a particular test system by its manufacturer.

To maintain speed characteristics for high count die contacts, the die contacts must be distributed throughout, or around the edges of the dice in a dense array. With this arrangement it is very difficult to parallel probe multiple dice using needle type probe cards, and impossible with dice having high count die contacts. Buckle beam probe cards are a costly alternative for probing dice having high count die contacts.

In view of the foregoing, improved probe cards capable of testing wafers with large numbers of dice, and high count die contacts, at high speeds, are needed in the art. In addition, probe cards capable of expanding tester resources to accommodate high parallelism, and high count die contact testing applications are needed in the art.

SUMMARY OF THE INVENTION

In accordance with the present invention, a probe card, a test system, and a test method for testing semiconductor dice contained on a wafer are provided. The probe card is adapted for use with a conventional tester and wafer prober. The probe card includes an on board multiplex circuit adapted to fan out, and selectively transmit, test signals from the tester to the wafer in response to control signals. The multiplex circuit includes active electrical switching devices, such as FETs, operable by control signals generated by a controller.

The multiplex circuit allows tester resources to be fanned out to multiple devices under test, while maintaining the uniqueness of each device, and the ability to disconnect failing devices. The additional control of the test signals also speeds up the testing process, and allows higher wafer throughputs using the same tester resources.

In addition to the multiplex circuit, the probe card includes a substrate, and a pattern of contacts formed on the substrate. During a test procedure, the probe card contacts make temporary electrical connections with die contacts on

US 6,300,786 B1

3

the wafer. Each probe card contact can be enabled or disabled as required by the multiplex circuit, to selectively write (send) the test signals to the die contacts, and to selectively read (receive) output signals from the die contacts.

The probe card and its contacts can be configured to electrically engage one die at a time, or multiple dice at the same time, up to all of the dice contained on the wafer. In an exemplary test procedure, dice can be tested for opens and shorts in groups corresponding to the available tester resources. Next, multiple dice can be written to in parallel by multiplexing drive only and I/O resources of the tester. Following the write step, multiple dice can be read in parallel in groups corresponding to the available tester drive only and I/O resources.

With the probe card comprising a semiconducting material such as silicon, the multiplex circuit can include integrated circuits and active electrical switching devices, formed directly on the substrate, using semiconductor circuit fabrication techniques. Alternately, the multiplex circuit can be fabricated on an interposer mounted to the probe card substrate, or on a die attached to the probe card substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a prior art semiconductor wafer containing multiple semiconductor dice;

FIG. 2 is a plan view of a prior art semiconductor die illustrating die contacts on a face of the die and exemplary functional designations for the die contacts;

FIG. 3 is a schematic cross sectional view of a test system constructed in accordance with the invention;

FIG. 4 is an enlarged plan view taken along section line 4—4 of FIG. 3 illustrating a probe card constructed in accordance with the invention;

FIG. 4A is an enlarged plan view equivalent to FIG. 4 of an alternate embodiment probe card;

FIG. 4B is a schematic cross sectional view of another alternate embodiment probe card;

FIG. 4C is a schematic cross sectional view of another alternate embodiment probe card;

FIG. 5A is an enlarged cross sectional view taken along section line 5A—5A of FIG. 4, following contact of the probe card and wafer, and illustrating probe card contacts electrically engaging die contacts on the wafer;

FIG. 5B is an enlarged cross sectional view taken along section line 5B—5B of FIG. 4, illustrating a FET transistor of on board circuitry contained on the probe card;

FIG. 5C is an enlarged cross sectional view taken along section line 5C—5C of FIG. 4 illustrating a bonding pad on the probe card;

FIG. 5D is an enlarged cross sectional view taken along section line 5D—5D of FIG. 4A illustrating an alternate embodiment probe card contact electrically engaging a die contact on the wafer;

FIG. 5E is an enlarged cross sectional view taken along section line 5E—5E of FIG. 4A illustrating an alternate embodiment probe card contact electrically engaging a bumped die contact on the wafer;

FIG. 6 is an enlarged view of a portion of FIG. 3 illustrating the probe card;

FIG. 7 is a block diagram illustrating steps in a method for testing in accordance with the invention;

FIG. 8A is a schematic electrical diagram of on board circuitry and a test site contained on the probe card and the electrical interface of the probe card and tester;

4

FIG. 8B is a schematic electrical diagram of a multiplex circuit of the on board circuitry;

FIG. 8C is a schematic electrical diagram illustrating a test operation for a tester with a prior art probe card; and

FIG. 8D is a schematic electrical diagram illustrating a test operation for the tester of FIG. 8C but with a probe card and multiplex circuit constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a prior art semiconductor wafer 10 includes multiple semiconductor dice 12 fabricated using processes that are well known in the art. As shown in FIG. 2, each die 12 includes multiple die contacts 14 formed thereon. The die contacts 14 comprise metal pads in electrical communication with integrated circuits contained on the die 12.

Following singulation of the wafer 10, the dice 12 can be packaged. In this case, the die contacts 14 can be wire bonded to lead fingers formed on a leadframe. The singulated dice 12 can also be used in unpackaged form as known good die (KGD). In this case, the die contacts 14 can be wire bonded to a substrate, such as a printed circuit board, or alternately flip chip mounted using reflowed solder bumps. The singulated dice 12 can also be included in chip scale packages. In this case, interconnects such as conductive bumps electrically contact the die contacts 14 to establish electrical communication with external contacts on a substrate.

For illustrative purposes, each die 12 includes twenty eight die contacts 14 with the functional designations indicated in FIG. 2. However, as is apparent, the number and functional arrangements of the die contacts 14 are merely exemplary, and other arrangements are possible.

Referring to FIG. 3, a test system 16 constructed in accordance with the invention, and configured to test the dice 12 contained on the wafer 10. The test system 16 includes a test head 30 and a probe card 20. The probe card 20 includes probe card contacts 22 configured to make temporary electrical connections with the die contacts 14. The test system 16 also includes a wafer prober 18 wherein the probe card 20 is mounted, and a tester 26 configured to apply test signals through the probe card 20, to the dice 12 contained on the wafer 10, and to analyze the resultant signals. The wafer prober 18 includes a probe card holder 62 for mounting and electrically interfacing with the probe card 20. Further details of the mounting of the probe card 20 to the test head 30 will be hereinafter described.

The wafer prober 18 includes a wafer chuck 24 configured to move in X and Y directions to align the wafer 10 with the probe card 20, and in the Z direction to move the wafer 10 into contact with the probe card 20. One suitable wafer prober 18 is manufactured by Electroglass and is designated a Model 4080.

The test system 16 also includes a prober interface board 28 for routing test signals from the test head 30 to the probe card 20. In addition, the prober interface board 28 can be in electrical communication with tester pin electronics 32 in the test head 30. The tester pin electronics 32 provide separate electrical paths 34 from test circuitry 33 contained in the tester 26, to the test head 30 and to the prober interface board 28.

The signal generating and analyzing capability of the test circuitry 33, and the number of separate electrical paths 34

US 6,300,786 B1

5

provided by the tester pin electronics 32, are termed herein as "tester resources". In general, the configurations of the test circuitry 33, and of the electrical paths 34, are fixed for a particular tester 26 by the manufacturer. For example, the test circuitry 33 can be configured to route drive only signals through some of the electrical paths 34, and input/output channels through other of the electrical paths 34, as required for testing a particular type of die 12. Exemplary testers 26 are commercially available from Teradyne of Boston Mass., as well as other manufacturers.

Referring to FIG. 4, further details of the probe card 20 are illustrated. The contacts 22 on the probe card 20 are arranged in patterns corresponding to the patterns of the die contacts 14. Each pattern of contacts 22 represents a single test site (S). For simplicity, only one pattern of contacts 22 and one test site (S) on the probe card 20 is illustrated. However, in actual practice, the probe card 20 can include multiple patterns of contacts 22 forming multiple test sites (S1 . . . Sn) to accommodate testing of multiple dice 12 at the same time. The contacts 22 on the test site S are designated 1-28 in correspondence with the die contacts 14 (FIG. 2).

In order to test multiple dice 12 at the same time certain conditions must be met. Firstly, the patterns of contacts 22 must exactly match the patterns of the die contacts 14. In addition, the stepping distance (i.e., x-y repeat and pattern spacing) must be the same for the contacts 22 as for the die contacts 14. Secondly, the software that controls the stepping process must be able to pick valid test sites. For example, when testing at the edges of a round wafer with a probe card that includes rectangular or square patterns of contacts 22, some patterns of contacts 22 will not have an associated device under test. It is also desirable to not have contacts 22 contacting a passivation layer 48 (FIG. 5A) on the dice 12 as this can damage the contacts 22.

In general, the use of the probe card 20 can greatly reduce the number of steps necessary for the prober 18 to test all of the dice 12 contained on the wafer 10. In the extreme case, rather than using stepping methods, the probe card 20 can be formed with enough patterns of contacts 22 to simultaneously contact every die contact 14 for all of the dice 12 on the wafer 10. Test signals can then be selectively applied and electronically switched as required, to selected dice 12 on the wafer 10. The probe card 20 can be formed with any desired number of test sites (S1 . . . Sn). In addition, the probe card 20 can be configured to test a complete semiconductor wafer 10, or to test a portion of the dice 12 in a partial wafer, or other substrate.

Still referring to FIG. 4, in addition to the patterns of contacts 22, the probe card 20 includes patterns of conductors 36 in electrical communication with the contacts 22 and with on-board circuitry 38. The contacts 22 and conductors 36 are formed on a substrate 40 of the probe card 20.

In the embodiment illustrated in FIG. 5A, the substrate 40 comprises silicon (or another semiconducting material such as gallium arsenide). This permits the on-board circuitry 38 to be formed as integrated circuits on the substrate 40 using semiconductor circuit fabrication techniques such as doping, CVD, photolithography, and etching. Also, with the substrate 40 comprising silicon, a coefficient of thermal expansion of the probe card 20 exactly matches that of the wafer 10. The substrate 40 can also comprise a silicon containing material, such as silicon-on-glass, and the on board circuitry can be formed on a layer of the substrate 40.

Preferably, the substrate 40 is thick enough to resist deflection and buckling during test procedures using the

6

probe card 20. In addition, an electrically insulating layer 42, such as SiO₂, polyimide, or BPSG can be formed on the substrate 40 to provide insulation for the contacts 22 and conductors 36 from the bulk of the substrate 40.

The conductors 36 on the substrate 40 are in electrical communication with the probe card contacts 22, and with the on board circuitry 38. The conductors 36 can be formed on a surface of the substrate 40 in a required pattern. In addition, the conductors 36 can include interlevel segments, such as metal vias or other interlevel electrical paths, that are in electrical communication with other components of the on-board circuitry 38.

In addition, the conductors 36 can be placed in electrical communication with the test circuitry 33 to provide electrical paths from the test circuitry 33 (FIG. 3) to the on-board circuitry 38, and to the contacts 22. Preferably, the conductors 36 comprise a highly conductive metal such as copper, aluminum, titanium, tantalum, tungsten, molybdenum or alloys of these metals. The conductors 36 can be formed as a single layer of metal, or as a multi metal stack, using a thin film metallization process (e.g., CVD, patterning, etching). Alternately, a thick film metallization process (e.g., screen printing, stenciling) can be used to form the conductors 36.

The conductors 36 also include bonding pads 44 located along the peripheral edges of the probe card 20. The bonding pads 44 provide bonding sites for forming separate electrical paths from the probe card holder 62 (FIG. 1) to each of the conductors 36. Preferably the bonding pads 44 are located on recessed surfaces 46 (FIG. 5C) along the edges of the substrate 40 to provide clearance for TAB bonds, wire bonds, spring loaded connectors (e.g., "POGO PINS") or other electrical connections to the bonding pads 44.

Referring to FIG. 5A, the probe card contacts 22 are shown in an enlarged cross sectional view. In the embodiment of FIG. 5A, the contacts 22 comprise raised members that project from a surface of the substrate 40. The raised contacts 22 help to provide a separation distance between the probe card 20 and the wafer 10 to clear any particulate contaminants that may be present on the opposing surfaces. In addition, the contacts 22 can include penetrating projections 50 adapted to penetrate the die contacts 14 to a limited penetration depth. To limit the penetration depth, the penetrating projections 50 have a height that is less than a thickness of the die contacts 14. For thin film aluminum die contacts 14, this thickness will typically be less than about 1.0 μ m. As also shown in FIG. 5A, surfaces 52 at the tips of the contacts 22 provide stop planes for limiting penetration of the contacts 22 into the die contacts 14. These stop plane surfaces 52 along with the dimensions of the penetrating projections 50 insures that the contacts 22 minimally damage the die contacts 14 during a test procedure.

The contacts 22 and penetrating projections 50 can be formed integrally with the substrate 40 using a bulk micro-machining process. With such a process, an etch mask (e.g., Si₃N₄ layer) can be formed on the substrate 40 and a suitable etchant, such as KOH, can be used to etch the substrate 40 to form the contacts 22. Solid areas of the etch mask determine the peripheral dimensions and shape of the contacts 22. The etch rate and time of the etch process determine the etch depth and the height of the contacts 22. Such a process permits the contacts 22, and penetrating projections 50, to be formed accurately, and in a dense array to accommodate testing of dense arrays of die contacts 14.

A representative height of the contacts 22 can be from 50 μ m to 100 μ m. A representative width of the contacts 22 on a side can be from 25 μ m to 80 μ m. A spacing of the contacts

US 6,300,786 B1

7

22 matches the spacing of the die contacts 14. A height of the penetrating projections 50 can be from about 2000 Å–5000 Å.

Still referring to FIG. 5A, each contact 22 is covered with a conductive layer 54 in electrical communication with a conductor 36. The conductive layers 54 for all of the contacts 22 can be formed of a metal layer deposited and patterned to cover the contacts 22, or other selected areas of the substrate 40. By way of example, the conductive layers 54 for the contacts 22 can comprise aluminum, copper, titanium, tungsten, tantalum, platinum, molybdenum, cobalt, nickel, gold, iridium or alloys of these metals. Some of these materials such as gold and platinum are non-reactive so that material transfer between the contacts 22 and the die contacts 14 can be minimized. The conductive layers 54 can also comprise a metal silicide or a conductive material such as doped polysilicon. Further, the conductive layers 54 can comprise a bi-metal stack including a base layer, and a non-reactive and oxidation resistant outer layer, such as gold or platinum.

The conductive layers 54 can be formed using a metallization process that includes blanket deposition (e.g., CVD), formation of a resist mask, and then etching. Preferably, the resist mask comprises a thick film resist that can be deposited to a thickness greater than a conventional resist. One suitable resist is a negative tone, thick film resist sold by Shell Chemical under the trademark "EPON RESIN SU-8".

The conductive layer 54 for each contact 22 is in electrical communication with a corresponding conductor 36 formed on the substrate 40. The conductive layers 54 and conductors 36 can be formed at the same time using the same metallization process. Alternately, the conductors 36 can be formed of a different metal than the conductive layers 54 using separate metallization process.

A process for fabricating the contacts 22 on a silicon substrate, substantially as shown in FIG. 5A is described in U.S. Pat. No. 5,483,741, entitled "METHOD FOR FABRICATING A SELF LIMITING SILICON BASED INTERCONNECT FOR TESTING BARE SEMICONDUCTOR DICE", and in U.S. Pat. No. 5,686,317 entitled "METHOD FOR FORMING AN INTERCONNECT HAVING A PENETRATION LIMITED CONTACT STRUCTURE FOR ESTABLISHING A TEMPORARY ELECTRICAL CONNECTION WITH A SEMICONDUCTOR DIE", both of which are incorporated herein by reference.

Referring to FIG. 5B, an enlarged cross sectional view of a FET transistor 100 of the on board circuitry 38 is illustrated. As is apparent the FET transistor 100 is merely one component of the on board circuitry 38. The on board circuitry 38 can include many FET transistors 100, as well as additional components, to provide the circuit arrangements that will be hereinafter explained. Further, other active electrical switching devices, such as NPN or PNP transistors can be used in place of the FET transistor 100 illustrated in the preferred embodiment.

The FET transistors 100 can be formed integrally with the substrate 40 using semiconductor circuit fabrication techniques. A suitable process sequence can include initially etching the contacts 22 (FIG. 5A) and penetrating projections 50 (FIG. 5A) and then fabricating the FET transistors 100. Following formation of the FET transistors 100, the insulating layer 42 can be formed, the conductive layers 54 (FIG. 5A) can be formed, and the conductors 36 can be formed. Each FET transistor 100 includes a polysilicon gate 102, and a gate oxide 104. In addition, a field oxide 106 is formed on the substrate 40 for electrically isolating the FET

8

transistors 100. The substrate 40 also includes N+ active areas 108, which can be formed by implanting dopants into the substrate 40 to form the sources and drains of the FET transistors 100. Metal filled vias 110 with metal silicide layers 112, electrically connect the sources and drains of the FET transistors 100 to the conductors 36. The FET transistors 100 also include spacers 114, TEOS layers 116 and nitride caps 118.

Referring to FIG. 4A, an alternate embodiment probe card 20A is illustrated. The probe card 20A is substantially similar to the probe card 20 previously described, but includes on board circuitry 38A formed on a surface of the substrate 40 rather than being formed integrally therewith. For example, the on board circuitry 38A can be included in a separate die mounted to the substrate 40, and then interconnected to the conductors 36. In this case the die containing the on board circuitry can be wire bonded or flip chip mounted to the substrate 40 in electrical communication with the contacts 14. In this embodiment the substrate 40 can comprise silicon, ceramic, or a glass filled resin (FR-4).

As another alternative, the on board circuitry can be included on an interposer attached to the probe card 20. Examples of interposers are shown in FIGS. 4B and 4C. In FIG. 4B, an interposer 84B includes on-board circuitry 38B, substantially as previously described. The interposer 84B can comprise a semiconducting material such as silicon, in which case the on-board circuitry 38B can be fabricated on the interposer 84B using semiconductor circuit fabrication techniques. Wire 88 can then be bonded to pads on the probe card 20 and to pads on the interposer 84A to provide separate electrical paths there between.

Alternately, as shown in FIG. 4C, on-board circuitry 38C can be contained on a die 86 attached to an interposer 84C (or directly to the probe card 20). In the embodiment of FIG. 4C, the die 86 is flip chip mounted to the interposer 84C. Reflowed solder bumps 90 on the die 86 are bonded to internal conductors 92 on the interposer 84C. In addition, the internal conductors 92 are in electrical communication with the contacts 22 on the probe card 20.

Referring to FIG. 5D, the probe card 20A can include contacts 22MB which are attached to the substrate 40 rather than being formed integrally therewith. As shown in FIG. 5D, the probe card contacts 22MB comprise metal microbumps formed on a polymer film 58 similar to multi layered TAB tape. In addition, conductors 36MB are formed on an opposing side of the polymer film 58 in electrical communication with the contacts 22MB. A compliant adhesive layer 60 attaches the polymer film 58 to a substrate 40MB. Further details of contact 22MB are described in U.S. Pat. No. 5,678,301, entitled "METHOD FOR FORMING AN INTERCONNECT FOR TESTING UNPACKAGED SEMICONDUCTOR DICE".

Another alternate embodiment probe card contact 22B is illustrated in FIG. 5E. Contacts 22B are configured to electrically engage die contacts 14B having solder bumps 56 formed thereon. The contacts 22B permit a bumped die 12B to be tested. The contacts 22B comprise indentations formed in a substrate 40B. In this embodiment the substrate can comprise silicon, gallium arsenide, ceramic or other substrate material. The indentations can be etched or machined to a required size and shape and then covered with conductive layers 54B. The contacts 22B are configured to retain the solder bumps 56. In addition, the conductive layers 54B for the contacts 22B are in electrical communication with conductors equivalent to the conductors 36 previously described. Further details of contact 22B are described in

US 6,300,786 B1

9

U.S. patent application Ser. No. 08/829,193, now U.S. Pat. No. 5,962,921, entitled "INTERCONNECT HAVING RECESSED CONTACT MEMBERS WITH PENETRATING BLADES FOR TESTING SEMICONDUCTOR DICE AND PACKAGES WITH CONTACT BUMPS", incorporated herein by reference.

Referring to FIG. 6, further details of the test system 16 and probe card 20 are illustrated. The wafer prober 18 includes the probe card holder 62, a force applying fixture 64 and a force applying mechanism 66. These items can be components of a conventional wafer prober as previously described. The force applying mechanism 66 presses against a pressure plate 68 and a compressible member 70 to bias the probe card 20 against the wafer 10. By way of example, the compressible member 70 can be formed of an elastomeric material such as silicone, butyl rubber, or fluorosilicone; in foam, gel, solid or molded configurations.

In addition, a flexible membrane 72 is bonded to the probe card 20 and to the probe card holder 62. In general, the flexible membrane 72 functions to physically attach the probe card 20 to the probe card holder 62. In addition, the flexible membrane 72 functions to provide electrical paths between the contacts 22 and the test circuitry 33 (FIG. 3) of the tester 26. The flexible membrane 72 can be formed of thin flexible materials to allow movement of the probe card 20 in Z-directions. For example, the flexible membrane 72 can be formed of a flexible multi layered material similar to TAB tape.

In the illustrative embodiment, the flexible membrane 72 comprises a layer of polymer tape having metal conductors thereon. Bonded connections are formed between the conductors on the membrane 72 and corresponding conductors 74 on the probe card holder 62. In addition, bonded connections are formed between the conductors on the membrane 72 and the bonding pads 44 on the probe card 20.

Still referring to FIG. 6, the wafer prober 18 includes spring loaded electrical connectors 76 which are in electrical communication with the probe interface board 28. One type of spring loaded electrical connector 76 is manufactured by Pogo Industries of Kansas City, Mo. under the trademark "POGO PINS". The electrical connectors 76 electrically communicate with internal conductors 78 on the probe card holder 62.

The probe card mounting arrangement shown in FIG. 6, as well as others, are described in U.S. patent application Ser. No. 08/797,719, entitled "PROBE CARD FOR SEMICONDUCTOR WAFERS AND METHOD AND SYSTEM FOR TESTING WAFERS", incorporated herein by reference. However, it is to be understood that these mounting arrangements are merely exemplary and the probe card 20 can be mounted in a conventional manner on a commercially available wafer prober.

Test Method

Referring to FIG. 7, steps in a method for testing the wafer 10 using the test system 18 and probe card 20 are illustrated. These steps are as follows.

1. Place contacts 22 on probe card 20 in electrical communication with die contacts 14 on dice 12 (devices under test).

2. Test the dice 12 in groups for opens and shorts by selectively actuating contacts 22 on the probe card 20 up to limit of tester resources.

3. Disable defective dice 12 by selectively actuating contacts 22 on the probe card 20.

4. Write test signals from tester 26 to multiple dice 12 by multiplexing input test signals to selected contacts 22 and die contacts 14 on multiple dice 12 at the same time.

10

5. Read test signals from multiple dice 12 in groups up to limit of tester resources, while maintaining device uniqueness and ability to disconnect defective dice 12.

Multiplex Circuit

Referring to FIGS. 8A-8D, further details of the on board circuitry 38 (FIG. 4A) are illustrated. In FIG. 8A a single test site S is illustrated. The test site S on the probe card 20 includes a pattern of contacts 22 which are configured to electrically engage die contacts 14 on a device under test DUT. As previously described, the probe card 20 is in electrical communication with the probe card holder 62, the tester pin electronics 32, and the test circuitry 33 within the tester 26.

As shown in FIG. 8A, the on board circuitry 38 includes a multiplex circuit 80. The multiplex circuit 80 is configured to receive test signals from the test circuitry 33 and to fan out or multiply the test signals. In addition, the multiplex circuit 80 is configured to selectively address the fanned out test signals through the probe card contacts 22 to selected die contacts 14 on the DUT. Stated differently, the multiplex circuit permits the test signals to be fanned out, allowing test procedures to be conducted in parallel. At the same time, the multiplex circuit 80 is configured to maintain the uniqueness of individual DUTs, and to electrically disconnect defective DUTs as required.

As shown in FIG. 8A, the multiplex circuit 80 includes a Util channel for each DUT, which functions as a control channel. In addition to the Util channel, the multiplex circuit 80 includes drive only channels, Vs channels, and I/O channels. The numbers of the channels are determined by the tester resources. Table I lists the tester resources of a model "J993" tester 26 manufactured by Teradyne.

TABLE I

Tester Resources of Teradyne "J993" Tester	
16 power supply channels per test head (30)	
16X, 16Y address generation channels per test head (30)	
16 DUTs can be tested in parallel per test head (30)	
72 I/O channels per test head (30)	
2 heads (30) per tester (26)	
320 drive only channels per head (30) divisible as follows:	
80 per test site (S) with 4 test sites (S0-S3)	
40 per test site (S) with 8 test sites (S0-S7)	
20 per test site (S) with 16 test sites (S0-S15)	
Up to 320 megabits of catch RAM	
36 Util channels per test head (30)	

Table II lists the tester resources of a model "J994" tester 26 manufactured by Teradyne.

TABLE II

Tester Resources of Teradyne "J994" Tester	
32 power supply channels per test head (30)	
16X, 16Y address generation channels per test head (30)	
32 DUTs can be tested in parallel per test head (30)	
144 I/O channels per test head (30)	
2 heads (30) per tester (26)	
640 drive only channels per head 30 divisible as follows:	
80 per test site (S) with 8 test sites (S1-S8)	
40 per test site (S) with 16 test sites (S1-S16)	
20 per test site (S) with 32 test sites (S1-S32)	
Up to 640 megabits of catch RAM	
52 Util channels per test head (30)	

US 6,300,786 B1

11

Table III lists the test requirements for one type of SRAM.

TABLE III

Sample SRAM Requirements For Each Device Under Test DUT
36 I/O channels per DUT
18 address channels (drive only) per DUT
32 control channels (drive only) per DUT
6 power supply channels (Vs-voltage supplies) per DUT
Util channels used depends on parallelism
Total
36 I/O channels per DUT
50 drive only channels per DUT
6 Vs channels per DUT

With these sample requirements a "J993" tester 26 can test two DUTs per test head 30, due to the I/O requirements. This is shown schematically in FIG. 8C. In FIG. 8C, the (J993) tester 26 includes a first test head 30-0 and a second test head 30-1. Each test head 30-0, 30-1, is capable of testing two DUTs, for a total of four at a time. Following testing of these four DUTs, both wafers 10 (one on each test head) can be stepped such that four additional DUTs align with the probe card contacts for testing.

A "J994" tester 26 has twice the tester resources of a "J993" tester 26. Accordingly on the basis of the above sample I/O requirements, a "J994" tester 26 can test four DUTs per test head 30, for a total of eight at a time.

Referring to FIG. 8B, a single test site S of the multiplex circuit 80 is illustrated. The multiplex circuit 80, simply stated, comprises multiple FET transistors 100 configured to provide a switching circuit for selectively enabling and disabling the contacts 22 on the probe card 20. The gate 102 of each FET transistor 100 is in electrical communication with the Util 0 channel. A controller 120 (or computer) generates control signals which are transmitted through the Util 0 channel to the FET transistors 100.

In the illustrative embodiment the multiplex circuit 80 is configured to test the SRAM of Table III. Accordingly, there are six Vs channels (Vs0 . . . Vs5), eighteen address channels (A0 . . . A17), and thirty six I/O channels (I/O0-I/O35). In addition, there is an OE channel, a CE channel, and an "all other controls" channel. With this arrangement test signals can be transmitted from the test circuitry 33 and latched by the channels. Control signals from the controller 120 then control the FET transistors 100 to enable and disable the contacts 22 to selectively transmit the test signals to the die contacts 14 as required.

During the test mode the uniqueness of each DUT is maintained. In addition, the control signals can be used operate the FET transistors 100 to disable selected contacts 22 in order to electrically disconnect defective DUTs. Still further, the control signals can be used to operate the FET transistors 100 to enable and disable selected contacts 22 in the transmission of "read" signals from the DUTs. However, in the "read" mode the DUTs must be read in accordance with the tester resources.

As is apparent, the multiplex circuit 80 illustrated in FIG. 8B is merely exemplary. Those skilled in the art, with the aid of the present specification, can design other multiplex circuits able to multiply and selectively address test signals from a tester. Thus other types of multiplexing circuits are intended to be included within the scope of the present claims.

Referring to FIG. 8D, the operation of the J993 tester 26 of Table I, outfitted with the probe card 20 having the multiplex circuit 80 is illustrated. In this example there are four test sites S0, S1, S2, S4 contained in two test heads

12

30-0, 30-1. Using the multiplex circuit each test site can write test signals to four DUTs at a time. In the "read" mode the additional three DUTs per test site must be selected in accordance with tester resources (e.g., one at a time or two at a time).

A limiting factor in the number of DUTs that can be tested by each test site is the drive current capacity of the channels of the tester 26. On the J993 and J994 testers 26, the drive current capacity is about 50 mA per channel. In addition, the test signals can be specified with a current (IOL) of about 8 mA per channel. Thus with some margin, each I/O channel and drive only channel of the tester 26 can be configured to drive four DUTs substantially as shown in FIG. 8D. During a write operation there is 8 mA per DUT×4 DUTs=32 mA per tester drive only channel. This leaves a 18 mA per channel margin.

Thus the invention provides an improved probe card for testing semiconductors wafers, a method for testing semiconductor wafers using the probe card, and a test system employing the probe card. The probe card can include contacts in dense arrays to accommodate testing of multiple dice having dense arrays of die contacts. In addition, the probe card includes on board circuitry configured to expand tester resources.

While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

What is claimed is:

1. A method for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts comprising:

providing a tester configured to transmit test signals to the dice on the wafer;

providing a probe card comprising a plurality of probe card contacts in electrical communication with the tester, the probe card contacts arranged in sets configured to electrically engage selected dice on the wafer; providing a multiplex circuit on the probe card in electrical communication with the probe card contacts and configured to selectively enable and disable the probe card contacts;

placing the probe card contacts in electrical communication with the die contacts on the wafer; and

using the multiplex circuit to control the test signals to fan out the test signals to the probe card contacts, to selectively transmit the test signals to the die contacts while the sets maintain a uniqueness of each die, and to disconnect defective dice.

2. The method of claim 1 wherein the probe card contacts comprise raised members at least partially covered with conductive layers.

3. The method of claim 1 wherein the probe card comprises silicon and the probe card contacts comprise etched members having projections configured to penetrate the die contacts.

4. The method of claim 1 wherein the probe card contacts comprise microbumps on a polymer film attached to the probe card.

5. The method of claim 1 wherein the die contacts comprise solder bumps, and the probe card contacts comprise indentations at least partially covered with conductive layers and configured to retain and electrically engage the solder bumps.

6. A method for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts comprising:

US 6,300,786 B1

13

providing a tester configured to transmit a write test signal to the dice;
providing a probe card comprising a plurality of probe card contacts in electrical communication with the tester, the probe card contacts arranged in sets configured to maintain a uniqueness of each die on the wafer;
providing a multiplex circuit on the probe card configured to control the test signals to fan out the write test signal into multiple write test signals and to selectively enable or disable the probe card contacts;
placing the probe card contacts in electrical communication with selected die contacts on the wafer;
writing the multiple write test signals to at least some of the selected die contacts at a same time by selective actuation of the probe card contacts;
reading a plurality of read test signals from the selected die contacts in groups by selective actuation of the probe card contacts; and
disabling at least some of the probe card contacts to disconnect any defective dice.
7. The method of claim 6 wherein the probe card comprises a semiconductor substrate and the multiplex circuit comprises a plurality of integrated circuits on the substrate.
8. The method of claim 6 further comprising providing a controller in electrical communication with the multiplex circuit configured to transmit control signals for controlling the multiplex circuit.
9. A method for testing semiconductor dice contained on a wafer comprising:
providing a tester comprising a test circuitry configured to generate and transmit write test signals to the dice and to analyze read test signals from the dice, the tester having tester resources determined by a signal generating, transmitting and analyzing capability of the test circuitry;
providing a probe card comprising an on-board multiplex circuit and a plurality of probe card contacts in electrical communication with the multiplex circuit and the tester, the multiplex circuit configured to control the test signals to speed up the testing, by fanning out the write test signals to multiple dice, and by reading the read test signals in groups up to a limit of the tester resources;

14

placing the probe card contacts in electrical communication with die contacts on selected dice;
writing the write test signals to the selected dice at a same time; and
reading the read test signals from the selected dice.
10. The method of claim 9 further comprising testing the die contacts on the selected dice for opens and shorts prior to the writing step.
11. The method of claim 9 further comprising following the reading step, disconnecting a defective die of the selected dice from the tester using the multiplex circuit.
12. A method for testing semiconductor dice contained on a wafer having a plurality of die contacts comprising:
providing a tester having a signal writing capability and a signal reading capability;
providing a probe card comprising a multiplex circuit and a plurality of probe card contacts in electrical communication with the multiplex circuit and the tester;
placing the probe card contacts in electrical communication with the die contacts on selected dice; and
using the multiplex circuit to control the test signals to expand the signal writing capability of the tester, and to speed up the testing, by multiplexing write test signals from the tester to the die contacts on the selected dice, by reading read test signals from the selected dice in groups up to the signal reading capability, and by controlling the probe card contacts to disable defective dice.
13. The method of claim 12 further comprising prior to the using step, testing the dice for opens and shorts in groups.
14. The method of claim 12 wherein the probe card comprises a silicon substrate and the multiplex circuit comprises a plurality of integrated circuits on the silicon substrate.
15. The method of claim 12 wherein the probe card contacts comprise projections configured to penetrate the die contacts.
16. The method of claim 12 wherein the die contacts comprise bumps and the probe card contacts comprise indentations configured to retain the bumps.

* * * * *



US006246250B1

(12) **United States Patent**
Doherty et al.

(10) **Patent No.: US 6,246,250 B1**
(45) **Date of Patent: *Jun. 12, 2001**

(54) **PROBE CARD HAVING ON-BOARD
MULTIPLEX CIRCUITRY FOR EXPANDING
TESTER RESOURCES**

(75) Inventors: **C. Patrick Doherty; Jorge L.
deVarona; Salman Akram**, all of
Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID
(US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

5,172,050	12/1992	Swapp	324/158 P
5,177,439	1/1993	Liu et al.	324/158 P
5,180,977	1/1993	Huff	324/158 P
5,225,037	7/1993	Elder et al.	156/644
5,264,787	11/1993	Woith et al.	324/158 P
5,323,107 *	6/1994	D'Souza	324/754
5,329,423	7/1994	Scholz	361/760
5,430,614	7/1995	Difrancesco	
5,483,741	1/1996	Akram et al.	29/846
5,625,298	4/1997	Hirano et al.	324/754
5,678,301	10/1997	Gochmour et al.	29/827
5,686,317	11/1997	Akram et al.	437/8
5,736,850 *	4/1998	Legal	324/158.1
5,869,974	2/1999	Akram et al.	
5,894,161	4/1999	Akram et al.	
5,952,840	9/1999	Farnworth et al.	
5,962,921	10/1999	Farnworth et al.	
6,048,750	4/2000	Hembree	
6,060,891	5/2000	Hembree et al.	
6,072,321	6/2000	Akram et al.	
6,078,186	6/2000	Hembree et al.	

* cited by examiner

(21) Appl. No.: **09/075,691**

(22) Filed: **May 11, 1998**

(51) Int. Cl.⁷ **G01R 31/26**

(52) U.S. Cl. **324/765; 324/754**

(58) Field of Search **324/754, 755,
324/757, 758, 765**

(56) **References Cited**

U.S. PATENT DOCUMENTS

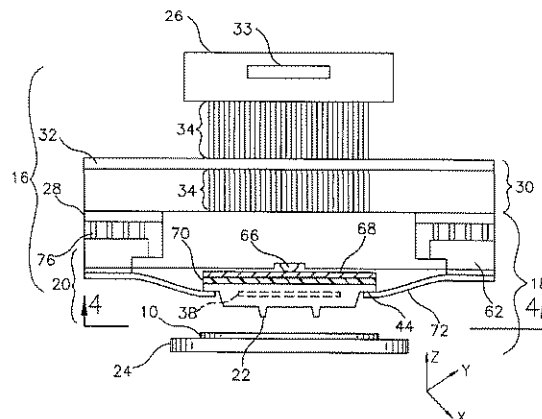
3,806,801	4/1974	Bove	324/72.5
4,027,935	6/1977	Byrnes et al.	339/48
4,585,991	4/1986	Reid et al.	324/158 P
4,891,585	1/1990	Janko et al.	324/158 P
4,906,920	3/1990	Huff et al.	324/158 P
4,918,383	4/1990	Huff et al.	324/158 F
4,954,458	9/1990	Reid	437/51
5,042,148	8/1991	Tada et al.	29/852
5,053,700 *	10/1991	Parrish	324/537
5,055,780 *	10/1991	Takagi et al.	324/765
5,070,297 *	12/1991	Kwon et al.	324/754
5,103,557 *	4/1992	Leedy	29/832
5,124,639	6/1992	Carlin et al.	324/158 P

Primary Examiner—Safet Metjahic
Assistant Examiner—Russell M. Kobert
(74) *Attorney, Agent, or Firm*—Stephen A. Gratton

(57) **ABSTRACT**

A probe card, a test method and a test system for testing semiconductor wafers are provided. The test system includes the probe card, a tester for generating test signals, and a wafer prober for placing the wafers and probe card in physical contact. The probe card includes contacts for electrically engaging die contacts on the wafer. The probe card also includes an on board multiplex circuit adapted to fan out and selectively transmit test signals from the tester to the probe card contacts. The multiplex circuit expands tester resources by allowing test signals to be written to multiple dice in parallel. Reading of the dice can be performed in groups up to the limit of the tester resources. In addition to expanding tester resources, the multiplex circuit maintains the individuality of each die, and permits defective dice to be electrically disconnected.

19 Claims, 7 Drawing Sheets



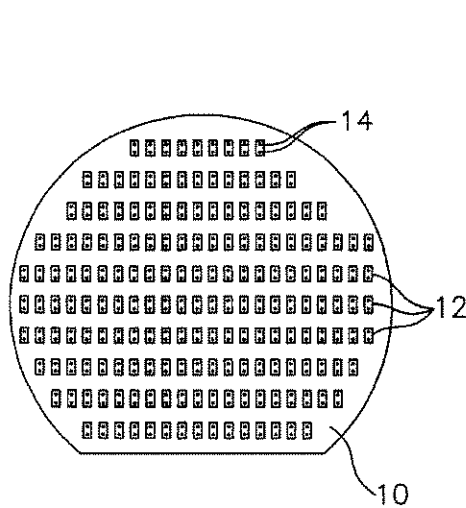


FIGURE 1
(PRIOR ART)

Vcc	1	28	Vss
DQ1	2	27	DQ8
DQ2	3	26	DQ7
DQ3	4	25	DQ6
DQ4	5	24	DQ5
NC	6	23	CAS
WE	7	22	OE
RAS	8	21	NC
A9	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

FIGURE 2
(PRIOR ART)

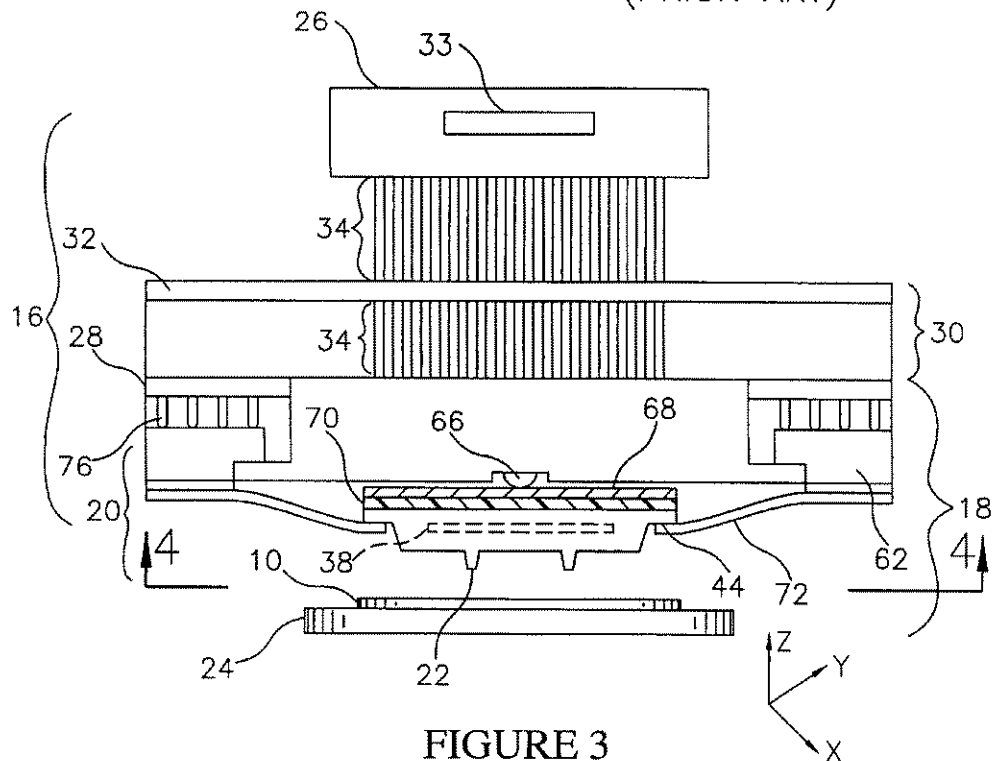


FIGURE 3

U.S. Patent

Jun. 12, 2001

Sheet 2 of 7

US 6,246,250 B1

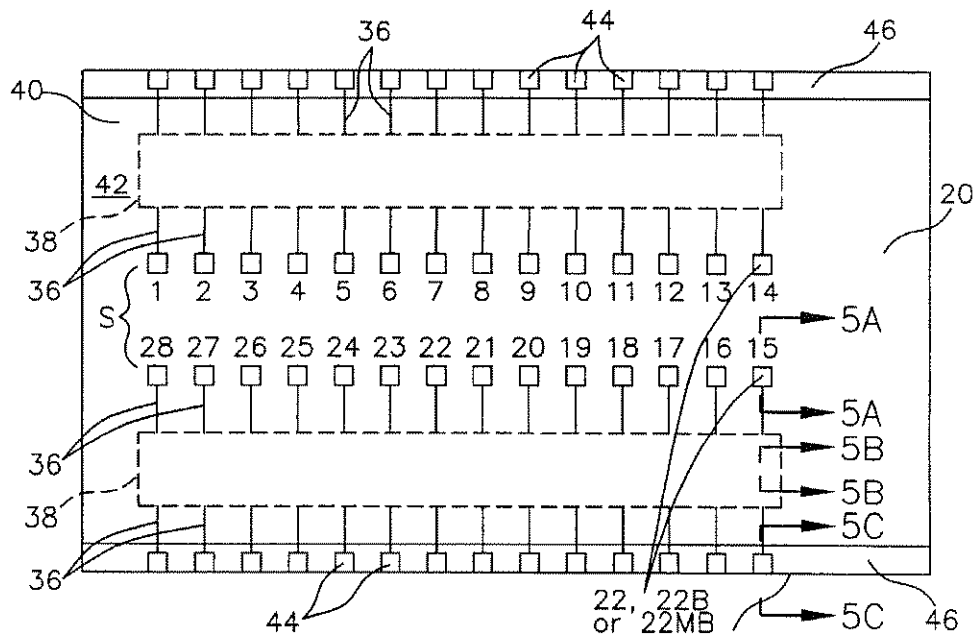


FIGURE 4

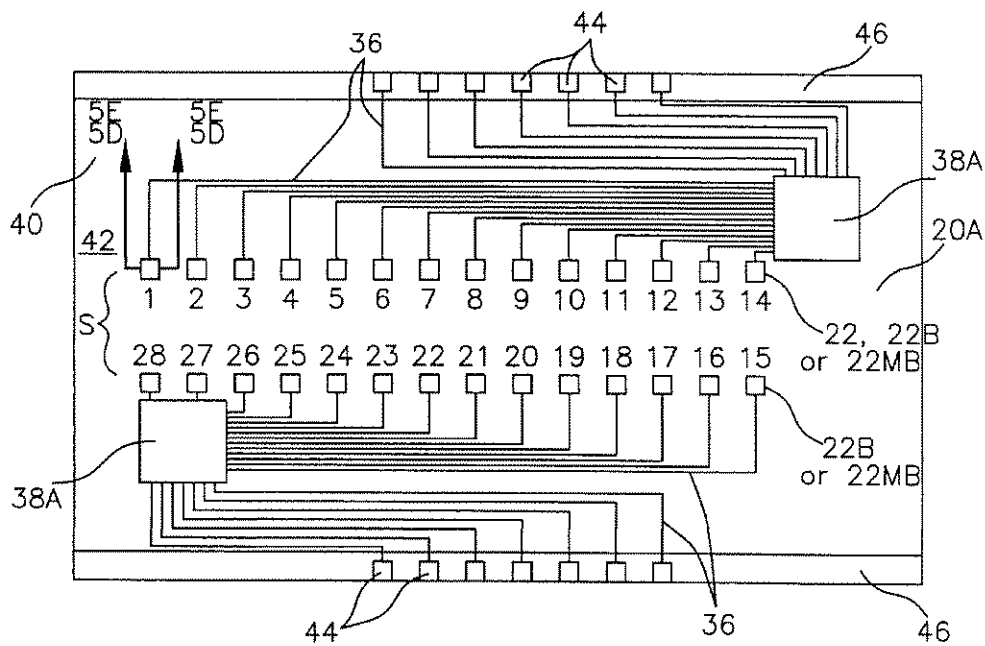


FIGURE 4A

U.S. Patent

Jun. 12, 2001

Sheet 3 of 7

US 6,246,250 B1

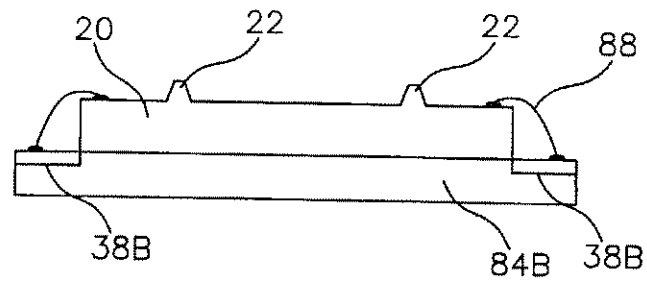


FIGURE 4B

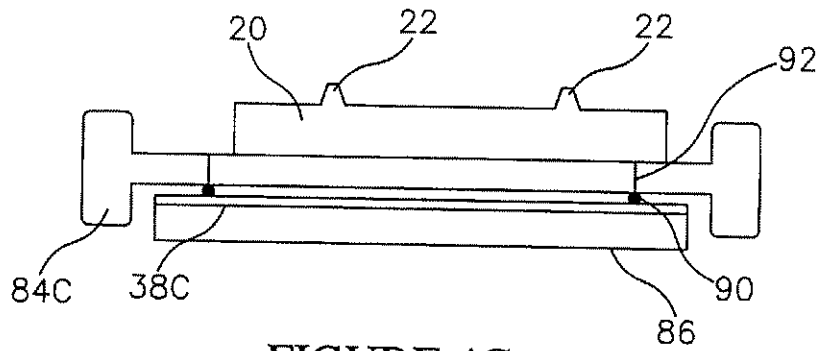


FIGURE 4C

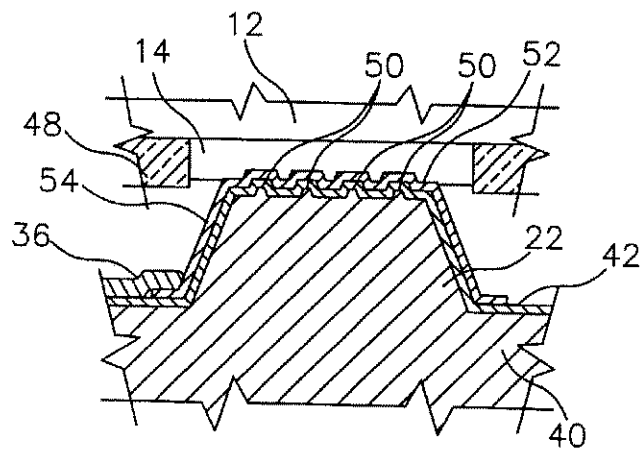


FIGURE 5A

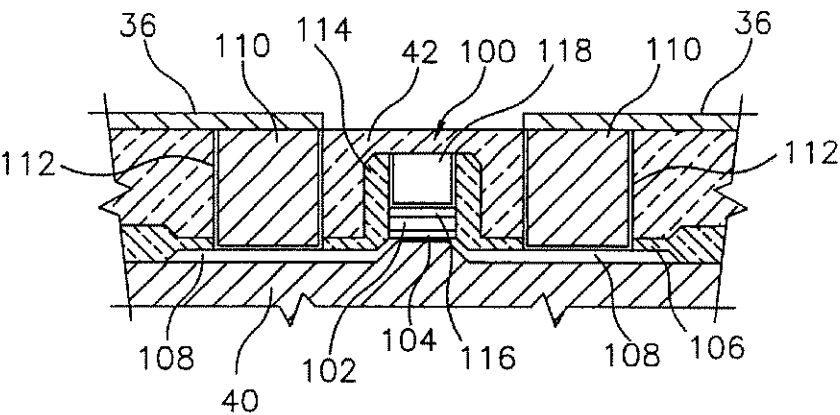


FIGURE 5B

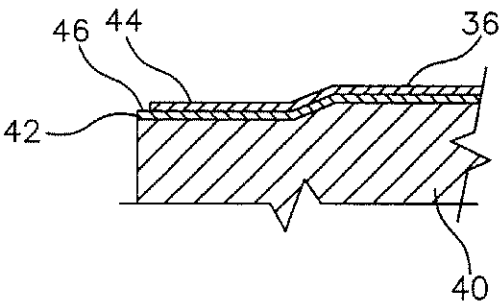


FIGURE 5C

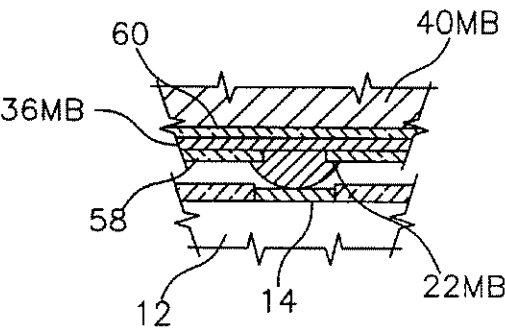


FIGURE 5D

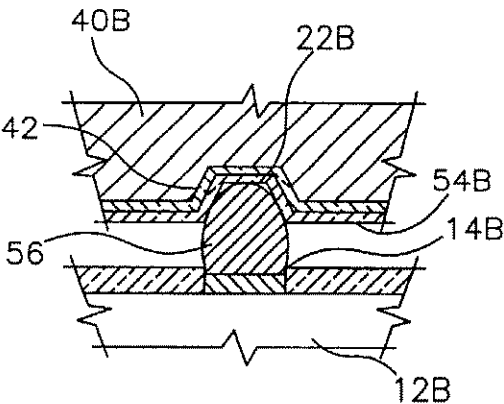


FIGURE 5E

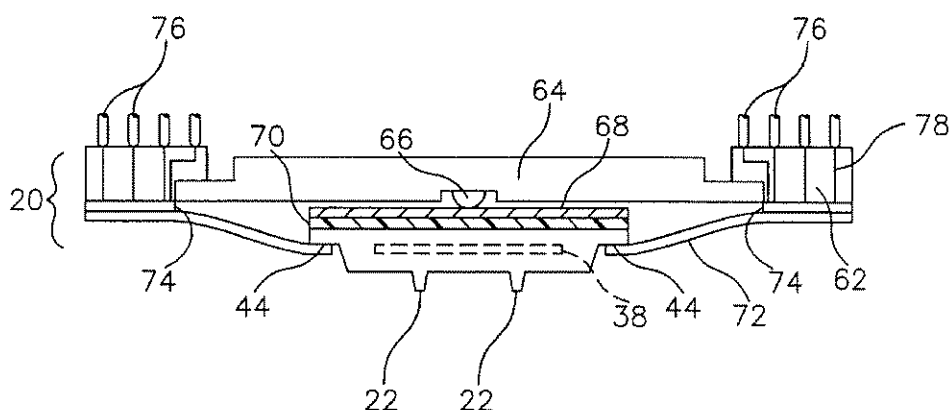


FIGURE 6

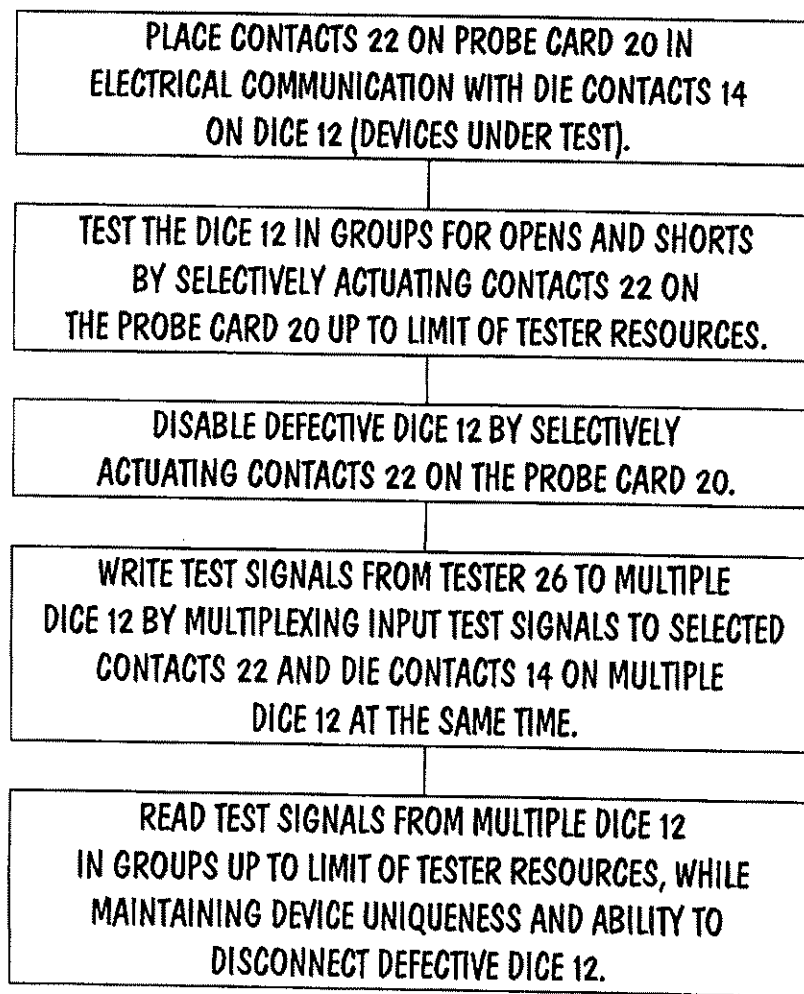


FIGURE 7

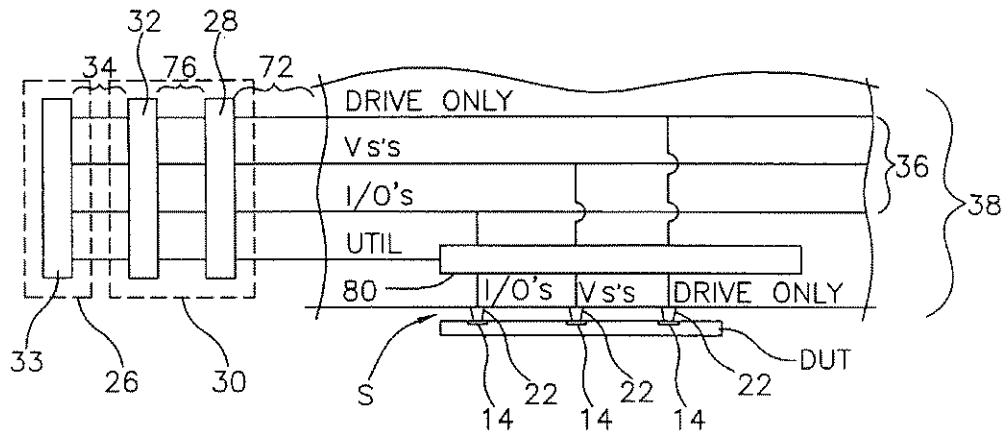


FIGURE 8A

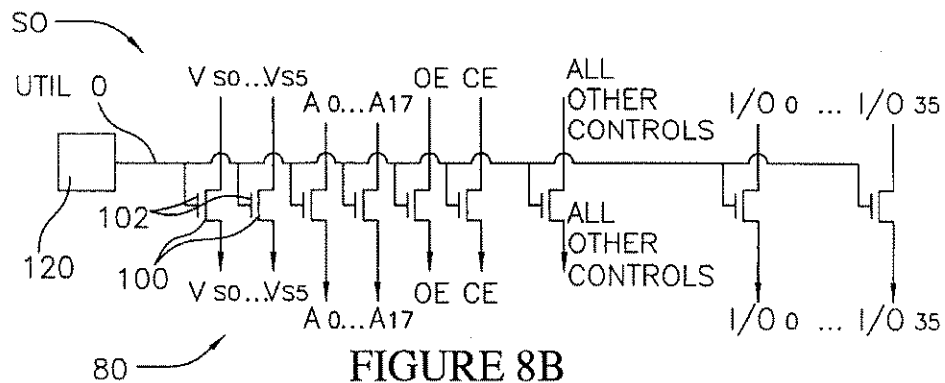


FIGURE 8B

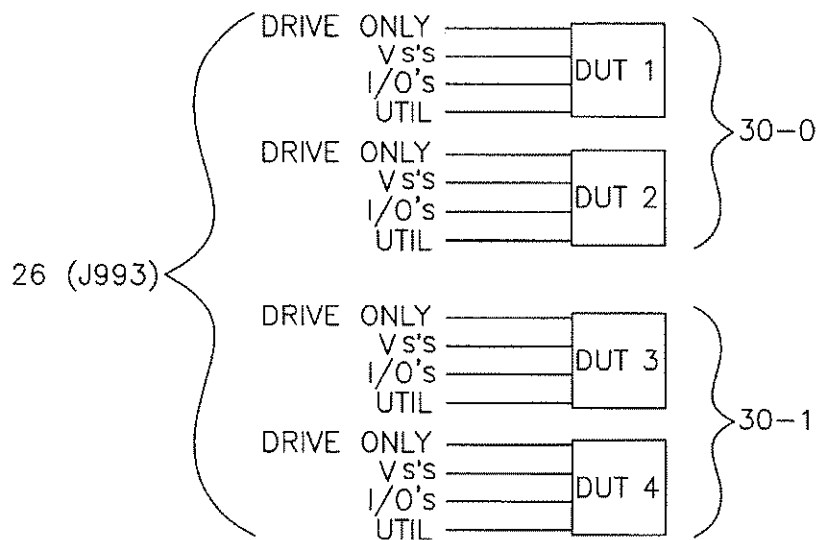


FIGURE 8C
(PRIOR ART)

U.S. Patent

Jun. 12, 2001

Sheet 7 of 7

US 6,246,250 B1

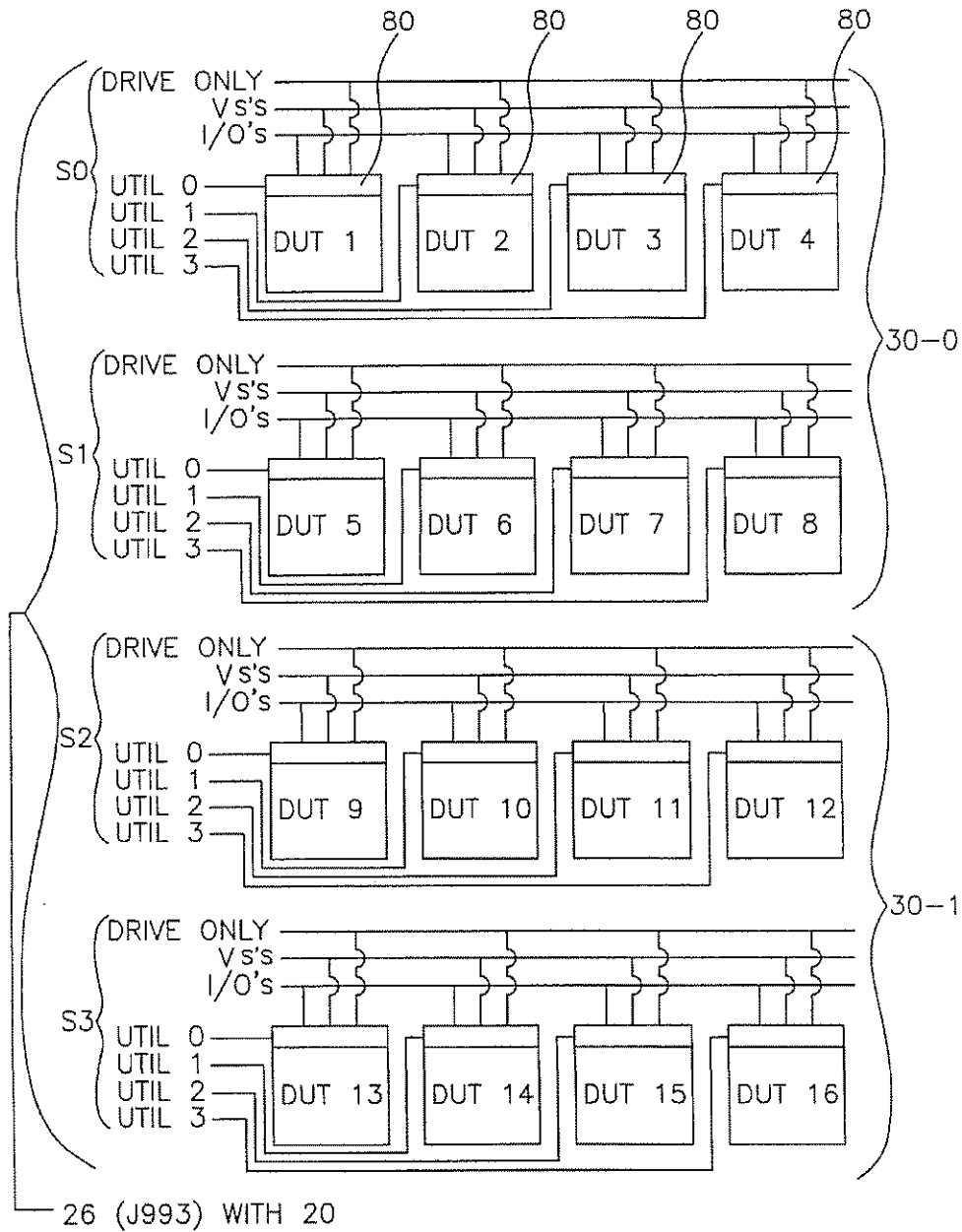


FIGURE 8D

US 6,246,250 B1

1

PROBE CARD HAVING ON-BOARD MULTIPLEX CIRCUITRY FOR EXPANDING TESTER RESOURCES

FIELD OF THE INVENTION

This invention relates generally to semiconductor manufacture and specifically to a probe card for testing semiconductor wafers. This invention also relates to test systems and test methods employing the probe card.

BACKGROUND OF THE INVENTION

Semiconductor wafers are tested prior to singulation into individual die, to assess the electrical characteristics of the integrated circuits contained on each die. A typical wafer-level test system includes a wafer prober for handling and positioning the wafers, a tester for generating test signals, a probe card for making temporary electrical connections with the wafer, and a prober interface board to route signals from the tester pin electronics to the probe card.

The test signals can include specific combinations of voltages and currents transmitted through the pin electronics channels of the tester to the probe interface board, to the probe card, and then to one or more devices under test on the wafer. During the test procedure response signals such as voltage, current and frequency can be analyzed and compared by the tester to required values. The integrated circuits that do not meet specification can be marked or mapped in software. Following testing, defective circuits can be repaired by actuating fuses to inactivate the defective circuitry and substitute redundant circuitry.

Different types of probe cards have been developed for probe testing semiconductor wafers. The most common type of probe card includes elongated needle probes configured to electrically engage die contacts, such as bond pads, or other contacts on the wafer. An exemplary probe card having needle probes is described in U.S. Pat. No. 4,563,640 to Hasegawa et al.

Although widely used, needle probe cards are difficult to maintain and unsuitable for high parallelism applications, in which multiple dice must be tested at the same time. In addition, needle probe cards are not suitable for some applications in which the dice have high count die contact requirements, such as bond pads in dense grid arrays. In particular, the long needles and variations in the needles lengths makes it difficult to apply a constant gram force to each die contact. Long needles can also generate parasitic signals at high speeds (e.g., >500 MHZ).

A similar type of probe card includes buckle beams adapted to flex upon contact with the wafer. This type of probe card is described in U.S. Pat. No. 4,027,935 to Byrnes et al. Although better for high count die contacts, and high parallelism applications, buckle beam probe cards are expensive, and difficult to maintain.

Another type of probe card, referred to as a "membrane probe card", includes a membrane formed of a thin and flexible dielectric material such as polyimide. An exemplary membrane probe card is described in U.S. Pat. No. 4,918,383 to Huff et al. With membrane probe cards, contact bumps are formed on the membrane in electrical communication with conductive traces, typically formed of copper.

One disadvantage of membrane contact bumps is that large vertical "overdrive" forces are required to penetrate oxide layers and make a reliable electrical connection with the die contacts on the dice. These forces can damage the die contacts and the dice. In addition, membrane probe cards

2

can be repeatedly stressed by the forces, causing the membrane to lose its resiliency. Use of high probe temperatures can also cause the membrane to lose resiliency.

Another disadvantage of membrane probe cards is the CTE (coefficient of thermal expansion) mismatch between the membrane probe card and wafer. In the future, with decreasing size of each die contact, higher parallelism requirements, and increased probing temperatures, maintaining electrical contact with the die contacts will be increasingly more difficult. In addition, because of relatively large differences between the CTE of membrane probe cards and silicon wafers, maintaining electrical contact between a large number of dice and a membrane probe card will be almost impossible.

Yet another limitation of conventional test systems, and a disadvantage of conventional probe cards, is that full functionality testing must be performed at the die level rather than at the wafer level. These tests require a large number of connections with the dice, and separate input/output paths between the dice and test circuitry. For functional test procedures on dice having multiple inputs and outputs, an input/output path must be provided to several die contacts at the same time. The number of dice that can be tested in parallel is always limited by the number of drive only, and input/output channels the tester provides, as well as the die contact arrangements on the dice. The number of drive only and input/output channels is fixed for a particular test system by its manufacturer.

To maintain speed characteristics for high count die contacts, the die contacts must be distributed throughout, or around the edges of the dice in a dense array. With this arrangement it is very difficult to parallel probe multiple dice using needle type probe cards, and impossible with dice having high count die contacts. Buckle beam probe cards are a costly alternative for probing dice having high count die contacts.

In view of the foregoing, improved probe cards capable of testing wafers with large numbers of dice, and high count die contacts, at high speeds, are needed in the art. In addition, probe cards capable of expanding tester resources to accommodate high parallelism, and high count die contact testing applications are needed in the art.

SUMMARY OF THE INVENTION

In accordance with the present invention, a probe card, a test system, and a test method for testing semiconductor dice contained on a wafer are provided. The probe card is adapted for use with a conventional tester and wafer prober. The probe card includes an on board multiplex circuit adapted to fan out, and selectively transmit, test signals from the tester to the wafer in response to control signals. The multiplex circuit includes active electrical switching devices, such as FETs, operable by control signals generated by a controller.

The multiplex circuit allows tester resources to be fanned out to multiple devices under test, while maintaining the uniqueness of each device, and the ability to disconnect failing devices. The additional control of the test signals also speeds up the testing process, and allows higher wafer throughputs using the same tester resources.

In addition to the multiplex circuit, the probe card includes a substrate, and a pattern of contacts formed on the substrate. During a test procedure, the probe card contacts make temporary electrical connections with die contacts on the wafer. Each probe card contact can be enabled or disabled as required by the multiplex circuit, to selectively write (send) the test signals to the die contacts, and to selectively read (receive) output signals from the die contacts.

US 6,246,250 B1

3

The probe card and its contacts can be configured to electrically engage one die at a time, or multiple dice at the same time, up to all of the dice contained on the wafer. In an exemplary test procedure, dice can be tested for opens and shorts in groups corresponding to the available tester resources. Next, multiple dice can be written to in parallel by multiplexing drive only and I/O resources of the tester. Following the write step, multiple dice can be read in parallel in groups corresponding to the available tester drive only and I/O resources.

With the probe card comprising a semiconducting material such as silicon, the multiplex circuit can include integrated circuits and active electrical switching devices, formed directly on the substrate, using semiconductor circuit fabrication techniques. Alternately, the multiplex circuit can be fabricated on an interposer mounted to the probe card substrate, or on a die attached to the probe card substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a prior art semiconductor wafer containing multiple semiconductor dice;

FIG. 2 is a plan view of a prior art semiconductor die illustrating die contacts on a face of the die and exemplary Ad functional designations for the die contacts;

FIG. 3 is a schematic cross sectional view of a test system constructed in accordance with the invention;

FIG. 4 is an enlarged plan view taken along section line 4—4 of FIG. 3 illustrating a probe card constructed in accordance with the invention;

FIG. 4A is an enlarged plan view equivalent to FIG. 4 of an alternate embodiment probe card;

FIG. 4B is a schematic cross sectional view of another alternate embodiment probe card;

FIG. 4C is a schematic cross sectional view of another alternate embodiment probe card;

FIG. 5A is an enlarged cross sectional view taken along section line 5A—5A of FIG. 4, following contact of the probe card and wafer, and illustrating probe card contacts electrically engaging die contacts on the wafer;

FIG. 5B is an enlarged cross sectional view taken along section line 5B—5B of FIG. 4, illustrating a FET transistor or on board circuitry contained on the probe card;

FIG. 5C is an enlarged cross sectional view taken along section line 5C—5C of FIG. 4 illustrating a bonding pad on the probe card;

FIG. 5E is an enlarged cross sectional view taken along section line 5E—5E of FIG. 4A illustrating an alternate embodiment probe card contact electrically engaging a bumped die contact on the wafer;

FIG. 5D is an enlarged cross sectional view taken along section line 5D—5D of FIG. 4A illustrating an alternate embodiment probe card contact electrically engaging a die contact on the wafer;

FIG. 6 is an enlarged view of a portion of FIG. 3 illustrating the probe card;

FIG. 7 is a block diagram illustrating steps in a method for testing in accordance with the invention;

FIG. 8A is a schematic electrical diagram of on board circuitry and a test site contained on the probe card and the electrical interface of the probe card and tester;

FIG. 8B is a schematic electrical diagram of a multiplex circuit of the on board circuitry;

FIG. 8C is a schematic electrical diagram illustrating a test operation for a tester with a prior art probe card; and

4

FIG. 8D is a schematic electrical diagram illustrating a test operation for the tester of FIG. 8C but with a probe card and multiplex circuit constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a prior art semiconductor wafer 10 includes multiple semiconductor dice 12 fabricated using processes that are well known in the art. As shown in FIG. 2, each die 12 includes multiple die contacts 14 formed thereon. The die contacts 14 comprise metal pads in electrical communication with integrated circuits contained on the die 12.

Following singulation of the wafer 10, the dice 12 can be packaged. In this case, the die contacts 14 can be wire bonded to lead fingers formed on a leadframe. The singulated dice 12 can also be used in unpackaged form as known good die (KGD). In this case, the die contacts 14 can be wire bonded to a substrate, such as a printed circuit board, or alternately flip chip mounted using reflowed solder bumps. The singulated dice 12 can also be included in chip scale packages. In this case, interconnects such as conductive bumps electrically contact the die contacts 14 to establish electrical communication with external contacts on a substrate.

For illustrative purposes, each die 12 includes twenty eight die contacts 14 with the functional designations indicated in FIG. 2. However, as is apparent, the number and functional arrangements of the die contacts 14 are merely exemplary, and other arrangements are possible.

Referring to FIG. 3, a test system 16 constructed in accordance with the invention, and configured to test the dice 12 contained on the wafer 10. The test system 16 includes a test head 30 and a probe card 20. The probe card 20 includes probe card contacts 22 configured to make temporary electrical connections with the die contacts 14. The test system 16 also includes a wafer prober 18 wherein the probe card 20 is mounted, and a tester 26 configured to apply test signals through the probe card 20, to the dice 12 contained on the wafer 10, and to analyze the resultant signals. The wafer prober 18 includes a probe card holder 62 for mounting and electrically interfacing with the probe card 20. Further details of the mounting of the probe card 20 to the test head 30 will be hereinafter described.

The wafer prober 18 includes a wafer chuck 24 configured to move in X and Y directions to align the wafer 10 with the probe card 20, and in the Z direction to move the wafer 10 into contact with the probe card 20. One suitable wafer prober 18 is manufactured by Electroglass and is designated a Model 4080.

The test system 16 also includes a prober interface board 28 for routing test signals from the test head 30 to the probe card 20. In addition, the prober interface board 28 can be in electrical communication with tester pin electronics 32 in the test head 30. The tester pin electronics 32 provide separate electrical paths 34 from test circuitry 33 contained in the tester 26, to the test head 30 and to the prober interface board 28.

The signal generating and analyzing capability of the test circuitry 33, and the number of separate electrical paths 34 provided by the tester pin electronics 32, are termed herein as "tester resources". In general, the configurations of the test circuitry 33, and of the electrical paths 34, are fixed for a particular tester 26 by the manufacturer. For example, the test circuitry 33 can be configured to route drive only signals

US 6,246,250 B1

5

through some of the electrical paths 34, and input/output channels through other of the electrical paths 34, as required for testing a particular type of die 12. Exemplary testers 26 are commercially available from Teradyne of Boston MA, as well as other manufacturers.

Referring to FIG. 4, further details of the probe card 20 are illustrated. The contacts 22 on the probe card 20 are arranged in patterns corresponding to the patterns of the die contacts 14. Each pattern of contacts 22 represents a single test site (S). For simplicity, only one pattern of contacts 22 and one test site (S) on the probe card 20 is illustrated. However, in actual practice, the probe card 20 can include multiple patterns of contacts 22 forming multiple test sites (S1 . . . Sn) to accommodate testing of multiple dice 12 at the same time. The contacts 22 on the test site S are designated 1-28 in correspondence with the die contacts 14 (FIG. 2).

In order to test multiple dice 12 at the same time certain conditions must be met. Firstly, the patterns of contacts 22 must exactly match the patterns of the die contacts 14. In addition, the stepping distance (i.e., x-y repeat and pattern spacing) must be the same for the contacts 22 as for the die contacts 14. Secondly, the software that controls the stepping process must be able to pick valid test sites. For example, when testing at the edges of a round wafer with a probe card that includes rectangular or square patterns of contacts 22, some patterns of contacts 22 will not have an associated device under test. It is also desirable to not have contacts 22 contacting a passivation layer 48 (FIG. 5A) on the dice 12 as this can damage the contacts 22.

In general, the use of the probe card 20 can greatly reduce the number of steps necessary for the prober 18 to test all of the dice 12 contained on the wafer 10. In the extreme case, rather than using stepping methods, the probe card 20 can be formed with enough patterns of contacts 22 to simultaneously contact every die contact 14 for all of the dice 12 on the wafer 10. Test signals can then be selectively applied and electronically switched as required, to selected dice 12 on the wafer 10. The probe card 20 can be formed with any desired number of test sites (S1 . . . Sn). In addition, the probe card 20 can be configured to test a complete semiconductor wafer 10, or to test a portion of the dice 12 in a partial wafer, or other substrate.

Still referring to FIG. 4, in addition to the patterns of contacts 22, the probe card 20 includes patterns of conductors 36 in electrical communication with the contacts 22 and with on-board circuitry 38. The contacts 22 and conductors 36 are formed on a substrate 40 of the probe card 20.

In the embodiment illustrated in FIG. 5A, the substrate 40 comprises silicon (or another semiconducting material such as gallium arsenide). This permits the on-board circuitry 38 to be formed as integrated circuits on the substrate 40 using semiconductor circuit fabrication techniques such as doping, CVD, photolithography, and etching. Also, with the substrate 40 comprising silicon, a coefficient of thermal expansion of the probe card 20 exactly matches that of the wafer 10. The substrate 40 can also comprise a silicon containing material, such as silicon-on-glass, and the on board circuitry can be formed on a layer of the substrate 40.

Preferably, the substrate 40 is thick enough to resist deflection and buckling during test procedures using the probe card 20. In addition, an electrically insulating layer 42, such as SiO₂, polyimide, or BPSG can be formed on the substrate 40 to provide insulation for the contacts 22 and conductors 36 from the bulk of the substrate 40.

The conductors 36 on the substrate 40 are in electrical communication with the probe card contacts 22, and with the

6

on board circuitry 38. The conductors 36 can be formed on a surface of the substrate 40 in a required pattern. In addition, the conductors 36 can include interlevel segments, such as metal vias or other interlevel electrical paths, that are in electrical communication with other components of the on-board circuitry 38.

In addition, the conductors 36 can be placed in electrical communication with the test circuitry 33 to provide electrical paths from the test circuitry 33 (FIG. 3) to the on-board circuitry 38, and to the contacts 22. Preferably, the conductors 36 comprise a highly conductive metal such as copper, aluminum, titanium, tantalum, tungsten, molybdenum or alloys of these metals. The conductors 36 can be formed as a single layer of metal, or as a multi metal stack, using a thin film metallization process (e.g., CVD, patterning, etching). Alternately, a thick film metallization process (e.g., screen printing, stenciling) can be used to form the conductors 36.

The conductors 36 also include bonding pads 44 located along the peripheral edges of the probe card 20. The bonding pads 44 provide bonding sites for forming separate electrical paths from the probe card holder 62 (FIG. 1) to each of the conductors 36. Preferably the bonding pads 44 are located on recessed surfaces 46 (FIG. 5C) along the edges of the substrate 40 to provide clearance for TAB bonds, wire bonds, spring loaded connectors (e.g., "POGO PINS") or other electrical connections to the bonding pads 44.

Referring to FIG. 5A, the probe card contacts 22 are shown in an enlarged cross sectional view. In the embodiment of FIG. 5A, the contacts 22 comprise raised members that project from a surface of the substrate 40. The raised contacts 22 help to provide a separation distance between the probe card 20 and the wafer 10 to clear any particulate contaminants that may be present on the opposing surfaces. In addition, the contacts 22 can include penetrating projections 50 adapted to penetrate the die contacts 14 to a limited penetration depth. To limit the penetration depth, the penetrating projections 50 have a height that is less than a thickness of the die contacts 14. For thin film aluminum die contacts 14, this thickness will typically be less than about 1.0 μ m. As also shown in FIG. 5A, surfaces 52 at the tips of the contacts 22 provide stop planes for limiting penetration of the contacts 22 into the die contacts 14. These stop plane surfaces 52 along with the dimensions of the penetrating projections 50 insures that the contacts 22 minimally damage the die contacts 14 during a test procedure.

The contacts 22 and penetrating projections 50 can be formed integrally with the substrate 40 using a bulk micro-machining process. With such a process, an etch mask (e.g., Si₃N₄ layer) can be formed on the substrate 40 and a suitable etchant, such as KOH, can be used to etch the substrate 40 to form the contacts 22. Solid areas of the etch mask determine the peripheral dimensions and shape of the contacts 22. The etch rate and time of the etch process determine the etch depth and the height of the contacts 22. Such a process permits the contacts 22, and penetrating projections 50, to be formed accurately, and in a dense array to accommodate testing of dense arrays of die contacts 14.

A representative height of the contacts 22 can be from 50 μ m to 100 μ m. A representative width of the contacts 22 on a side can be from 25 μ m to 80 μ m. A spacing of the contacts 22 matches the spacing of the die contacts 14. A height of the penetrating projections 50 can be from about 2000 Å-5000 Å.

Still referring to FIG. 5A, each contact 22 is covered with a conductive layer 54 in electrical communication with a conductor 36. The conductive layers 54 for all of the

US 6,246,250 B1

7

contacts 22 can be formed of a metal layer deposited and patterned to cover the contacts 22, or other selected areas of the substrate 40. By way of example, the conductive layers 54 for the contacts 22 can comprise aluminum, copper, titanium, tungsten, tantalum, platinum, molybdenum, cobalt, nickel, gold, iridium or alloys of these metals. Some of these materials such as gold and platinum are non-reactive so that material transfer between the contacts 22 and the die contacts 14 can be minimized. The conductive layers 54 can also comprise a metal silicide or a conductive material such as doped polysilicon. Further, the conductive layers 54 can comprise a bi-metal stack including a base layer, and a non-reactive and oxidation resistant outer layer, such as gold or platinum.

The conductive layers 54 can be formed using a metallization process that includes blanket deposition (e.g., CVD), formation of a resist mask, and then etching. Preferably, the resist mask comprises a thick film resist that can be deposited to a thickness greater than a conventional resist. One suitable resist is a negative tone, thick film resist sold by Shell Chemical under the trademark "EPON RESIN SU-8".

The conductive layer 54 for each contact 22 is in electrical communication with a corresponding conductor 36 formed on the substrate 40. The conductive layers 54 and conductors 36 can be formed at the same time using the same metallization process. Alternately, the conductors 36 can be formed of a different metal than the conductive layers 54 using separate metallization process.

A process for fabricating the contacts 22 on a silicon substrate, substantially as shown in FIG. 5A is described in U.S. Pat. No. 5,483,741, entitled "METHOD FOR FABRICATING A SELF LIMITING SILICON BASED INTERCONNECT FOR TESTING BARE SEMICONDUCTOR DICE", and in U.S. Pat. No. 5,686,317 entitled "METHOD FOR FORMING AN INTERCONNECT HAVING A PENETRATING LIMITED CONTACT STRUCTURE FOR ESTABLISHING A TEMPORARY ELECTRICAL CONNECTION WITH A SEMICONDUCTOR DIE", both of which are incorporated herein by reference.

Referring to FIG. 5B, an enlarged cross sectional view of a FET transistor 100 of the on board circuitry 38 is illustrated. As is apparent the FET transistor 100 is merely one component of the on board circuitry 38. The on board circuitry 38 can include many FET transistors 100, as well as additional components, to provide the circuit arrangements that will be hereinafter explained. Further, other active electrical switching devices, such as NPN or PNP transistors can be used in place of the FET transistor 100 illustrated in the preferred embodiment.

The FET transistors 100 can be formed integrally with the substrate 40 using semiconductor circuit fabrication techniques. A suitable process sequence can include initially etching the contacts 22 (FIG. 5A) and penetrating projections 50 (FIG. 5A) and then fabricating the FET transistors 100. Following formation of the FET transistors 100, the insulating layer 42 can be formed, the conductive layers 54 (FIG. 5A) can be formed, and the conductors 36 can be formed. Each FET transistor 100 includes a polysilicon gate 102, and a gate oxide 104. In addition, a field oxide 106 is formed on the substrate 40 for electrically isolating the FET transistors 100. The substrate 40 also includes N+ active areas 108, which can be formed by implanting dopants into the substrate 40 to form the sources and drains of the FET transistors 100. Metal filled vias 110 with metal silicide layers 112, electrically connect the sources and drains of the FET transistors 100 to the conductors 36. The FET transis-

8

tors 100 also include spacers 114, TEOS layers 116 and nitride caps 118.

Referring to FIG. 4A, an alternate embodiment probe card 20A is illustrated. The probe card 20A is substantially similar to the probe card 20 previously described, but includes on board circuitry 38A formed on a surface of the substrate 40 rather than being formed integrally therewith. For example, the on board circuitry 38A can be included in a separate die mounted to the substrate 40, and then interconnected to the conductors 36. In this case the die containing the on board circuitry can be wire bonded or flip chip mounted to the substrate 40 in electrical communication with the contacts 14. In this embodiment the substrate 40 can comprise silicon, ceramic, or a glass filled resin (FR-4).

As another alternative, the on board circuitry can be included on an interposer attached to the probe card 20. Examples of interposers are shown in FIGS. 4B and 4C. In FIG. 4B, an interposer 84B includes on-board circuitry 38B, substantially as previously described. The interposer 84B can comprise a semiconducting material such as silicon, in which case the on-board circuitry 38B can be fabricated on the interposer 84B using semiconductor circuit fabrication techniques. Wire 88 can then be bonded to pads on the probe card 20 and to pads on the interposer 84A to provide separate electrical paths there between.

Alternately, as shown in FIG. 4C, on-board circuitry 38C can be contained on a die 86 attached to an interposer 84C (or directly to the probe card 20). In the embodiment of FIG. 4C, the die 86 is flip chip mounted to the interposer 84C. Reflowed solder bumps 90 on the die 86 are bonded to internal conductors 92 on the interposer 84C. In addition, the internal conductors 92 are in electrical communication with the contacts 22 on the probe card 20.

Referring to FIG. 5D, the probe card 20A can include contacts 22MB which are attached to the substrate 40 rather than being formed integrally therewith. As shown in FIG. 5D, the probe card contacts 22MB comprise metal microbumps formed on a polymer film 58 similar to multi layered TAB tape. In addition, conductors 36MB are formed on an opposing side of the polymer film 58 in electrical communication with the contacts 22MB. A compliant adhesive layer 60 attaches the polymer film 58 to a substrate 40MB. Further details of contact 22MB are described in U.S. Pat. No. 5,678,301, entitled "METHOD FOR FORMING AN INTERCONNECT FOR TESTING UNPACKAGED SEMICONDUCTOR DICE".

Another alternate embodiment probe card contact 22B is illustrated in FIG. 5E. Contacts 22B are configured to electrically engage die contacts 14B having solder bumps 56 formed thereon. The contacts 22B permit a bumped die 12B to be tested. The contacts 22B comprise indentations formed in a substrate 40B. In this embodiment the substrate can comprise silicon, gallium arsenide, ceramic or other substrate material. The indentations can be etched or machined to a required size and shape and then covered with conductive layers 54B. The contacts 22B are configured to retain the solder bumps 56. In addition, the conductive layers 54B for the contacts 22B are in electrical communication with conductors equivalent to the conductors 36 previously described. Further details of contact 22B are described in U.S. Pat. No. 5,962,921, entitled "INTERCONNECT HAVING RECESSED CONTACT MEMBERS WITH PENETRATING BLADES FOR TESTING SEMICONDUCTOR DICE AND PACKAGES WITH CONTACT BUMPS", incorporated herein by reference.

Referring to FIG. 6, further details of the test system 16 and probe card 20 are illustrated. The wafer prober 18

includes the probe card holder 62, a force applying fixture 64 and a force applying mechanism 66. These items can be components of a conventional wafer prober as previously described. The force applying mechanism 66 presses against a pressure plate 68 and a compressible member 70 to bias the probe card 20 against the wafer 10. By way of example, the compressible member 70 can be formed of an elastomeric material such as silicone, butyl rubber, or fluorosilicone; in foam, gel, solid or molded configurations.

In addition, a flexible membrane 72 is bonded to the probe card 20 and to the probe card holder 62. In general, the flexible membrane 72 functions to physically attach the probe card 20 to the probe card holder 62. In addition, the flexible membrane 72 functions to provide electrical paths between the contacts 22 and the test circuitry 33 (FIG. 3) of the tester 26. The flexible membrane 72 can be formed of thin flexible materials to allow movement of the probe card 20 in Z-directions. For example, the flexible membrane 72 can be formed of a flexible multi layered material similar to TAB tape.

In the illustrative embodiment, the flexible membrane 72 comprises a layer of polymer tape having metal conductors thereon. Bonded connections are formed between the conductors on the membrane 72 and corresponding conductors 74 on the probe card holder 62. In addition, bonded connections are formed between the conductors on the membrane 72 and the bonding pads 44 on the probe card 20.

Still referring to FIG. 6, the wafer prober 18 includes spring loaded electrical connectors 76 which are in electrical communication with the prober interface board 28. One type of spring loaded electrical connector 76 is manufactured by Pogo Industries of Kansas City, Mo. under the trademark "POGO PINS". The electrical connectors 76 electrically communicate with internal conductors 78 on the probe card holder 62.

The probe card mounting arrangement shown in FIG. 6, as well as others, are described in U.S. Pat. No. 6,060,891, entitled "PROBE CARD FOR SEMICONDUCTOR WAFERS AND METHOD AND SYSTEM FOR TESTING WAFERS", incorporated herein by reference. However, it is to be understood that these mounting arrangements are merely exemplary and the probe card 20 can be mounted in a conventional manner on a commercially available wafer prober.

TEST METHOD

Referring to FIG. 7, steps in a method for testing the wafer 10 using the test system 18 and probe card 20 are illustrated. These steps are as follows.

1. Place contacts 22 on probe card 20 in electrical communication with die contacts 14 on dice 12 (devices under test).
 2. Test the dice 12 in groups for opens and shorts by selectively actuating contacts 22 on the probe card 20 up to limit of tester resources.
 3. Disable defective dice 12 by selectively actuating contacts 22 on the probe card 20.
 4. Write test signals from tester 26 to multiple dice 12 by multiplexing input test signals to selected contacts 22 and die contacts 14 on multiple dice 12 at the same time.
 5. Read test signals from multiple dice 12 in groups up to limit of tester resources, while maintaining device uniqueness and ability to disconnect defective dice 12.
- Multiplex Circuit

Referring to FIGS. 8A-8D, further details of the on board circuitry 38 (FIG. 4A) are illustrated. In FIG. 8A a single test

site S is illustrated. The test site S on the probe card 20 includes a pattern of contacts 22 which are configured to electrically engage die contacts 14 on a device under test DUT. As previously described, the probe card 20 is in electrical communication with the probe card holder 62, the tester pin electronics 32, and the test circuitry 33 within the tester 26.

As shown in FIG. 8A, the on board circuitry 38 includes a multiplex circuit 80. The multiplex circuit 80 is configured to receive test signals from the test circuitry 33 and to fan out or multiply the test signals. In addition, the multiplex circuit 80 is configured to selectively address the fanned out test signals through the probe card contacts 22 to selected die contacts 14 on the DUT. Stated differently, the multiplex circuit permits the test signals to be fanned out, allowing test procedures to be conducted in parallel. At the same time, the multiplex circuit 80 is configured to maintain the uniqueness of individual DUTs, and to electrically disconnect defective DUTs as required.

As shown in FIG. 8A, the multiplex circuit 80 includes a Util channel for each DUT, which functions as a control channel. In addition to the Util channel, the multiplex circuit 80 includes drive only channels, Vs channels, and I/O channels. The numbers of the channels are determined by the tester resources. Table I lists the tester resources of a model "J993" tester 26 manufactured by Teradyne.

TABLE I

Tester Resources of Teradyne "J993" Tester	
16 power supply channels per test head (30)	
16X, 16Y address generation channels per test head (30)	
16 DUTs can be tested in parallel per test head (30)	
72 I/O channels per test head (30)	
2 heads (30) per tester (26)	
320 drive only channels per head (30) divisible as follows:	
80 per test site (S) with 4 test sites (S0-S3)	
40 per test site (S) with 8 test sites (S-S7)	
20 per test site (S) with 16 test sites (S0-S15)	
Up to 320 megabits of catch RAM	
36 Util channels per test head (30)	

Table II lists the tester resources of a model "J994" tester 26 manufactured by Teradyne.

TABLE II

Tester Resources of Teradyne "J994" Tester	
32 power supply channels per test head (30)	
16X, 16Y address generation channels per test head (30)	
32 DUTs can be tested in parallel per test head (30)	
144 I/O channels per test head (30)	
2 heads (30) per tester (26)	
640 drive only channels per head 30 divisible as follows:	
80 per test site (S) with 8 test sites (S1-S8)	
40 per test site (S) with 16 test sites (S1-S16)	
20 per test site (S) with 32 test sites (S1-S32)	
Up to 640 megabits of catch RAM	
52 Util channels per test head (30)	

US 6,246,250 B1

11

Table III lists the test requirements for one type of SRAM.

TABLE III

Sample SRAM Requirements For Each Device Under Test DUT
36 I/O channels per DUT
18 address channels (drive only) per DUT
32 control channels (drive only) per DUT
6 power supply channels (Vs-voltage supplies) per DUT
Util channels used depends on parallelism
Total
36 I/O channels per DUT
50 drive only channels per DUT
6 Vs channels per DUT

With these sample requirements a "J993" tester 26 can test two DUTs per test head 30, due to the I/O requirements. This is shown schematically in FIG. 8C. In FIG. 8C, the (J993) tester 26 includes a first test head 30-0 and a second test head 30-1. Each test head 30-0, 30-1, is capable of testing two DUTs, for a total of four at a time. Following testing of these four DUTs, both wafers 10 (one on each test head) can be stepped such that four additional DUTs align with the probe card contacts for testing.

A "J994" tester 26 has twice the tester resources of a "J993" tester 26. Accordingly on the basis of the above sample I/O requirements, a "J994" tester 26 can test four DUTs per test head 30, for a total of eight at a time.

Referring to FIG. 8B, a single test site S of the multiplex circuit 80 is illustrated. The multiplex circuit 80, simply stated, comprises multiple FET transistors 100 configured to provide a switching circuit for selectively enabling and disabling the contacts 22 on the probe card 20. The gate 102 of each FET transistor 100 is in electrical communication with the Util 0 channel. A controller 120 (or computer) generates control signals which are transmitted through the Util 0 channel to the FET transistors 100.

In the illustrative embodiment the multiplex circuit 80 is configured to test the SRAM of Table III. Accordingly, there are six Vs channels (Vs0 . . . Vs5), eighteen address channels (A0 . . . A17), and thirty six I/O channels (I/O0-I/O35). In addition, there is an OE channel, a CE channel, and an "all other controls" channel. With this arrangement test signals can be transmitted from the test circuitry 33 and latched by the channels. Control signals from the controller 120 then control the FET transistors 100 to enable and disable the contacts 22 to selectively transmit the test signals to the die contacts 14 as required.

During the test mode the uniqueness of each DUT is maintained. In addition, the control signals can be used operate the FET transistors 100 to disable selected contacts 22 in order to electrically disconnect defective DUTs. Still further, the control signals can be used to operate the FET transistors 100 to enable and disable selected contacts 22 in the transmission of "read" signals from the DUTs. However, in the "read" mode the DUTs must be read in accordance with the tester resources.

As is apparent, the multiplex circuit 80 illustrated in FIG. 8B is merely exemplary. Those skilled in the art, with the aid of the present specification, can design other multiplex circuits able to multiply and selectively address test signals from a tester. Thus other types of multiplexing circuits are intended to be included within the scope of the present claims.

Referring to FIG. 8D, the operation of the J993 tester 26 of Table I, outfitted with the probe card 20 having the multiplex circuit 80 is illustrated. In this example there are four test sites S0, S1, S2, S4 contained in two test heads

12

30-0, 30-1. Using the multiplex circuit each test site can write test signals to four DUTs at a time. In the "read" mode the additional three DUTs per test site must be selected in accordance with tester resources (e.g., one at a time or two at a time).

A limiting factor in the number of DUTs that can be tested by each test site is the drive current capacity of the channels of the tester 26. On the J993 and J994 testers 26, the drive current capacity is about 50 mA per channel. In addition, the test signals can be specified with a current (IOL) of about 8 mA per channel. Thus with some margin, each I/O channel and drive only channel of the tester 26 can be configured to drive four DUTs substantially as shown in FIG. 8D. During a write operation there is 8 mA per DUT×4 DUTs=32 mA per tester drive only channel. This leaves a 18mA per channel margin.

Thus the invention provides an improved probe card for testing semiconductors wafers, a method for testing semiconductor wafers using the probe card, and a test system employing the probe card. The probe card can include contacts in dense arrays to accommodate testing of multiple dice having dense arrays of die contacts. In addition, the probe card includes on board circuitry configured to expand tester resources.

While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

What is claimed is:

1. A probe card for testing a semiconductor wafer having a plurality of wafer contacts comprising:
 - a substrate comprising a semiconductor material;
 - a plurality of contacts on the substrate configured to make temporary electrical connections with the wafer contacts, the contacts comprising raised portions of the substrate, projections on the raised portions for penetrating the wafer contacts, and conductive layers on the projections for electrically contacting the wafer contacts; and
 - a multiplex circuit comprising a plurality of integrated circuits integral with the substrate including a plurality of active electrical switching devices in electrical communication with the contacts, the circuit configured to fan out test signals from a tester, and to control the contacts to selectively transmit the test signals to the wafer contacts.
2. The probe card of claim 1 wherein the semiconductor material comprises silicon.
3. A probe card for testing a semiconductor wafer having a plurality of wafer contacts comprising:
 - a substrate comprising a semiconductor material;
 - a plurality of contacts on the substrate configured to make temporary electrical connections with the wafer contacts; and
 - a multiplex circuit comprising a plurality of integrated circuits integral with the substrate including a plurality of active electrical switching devices on the substrate in electrical communication with the contacts, and configured to fan out test signals from a tester, the multiplex circuit operable in response to control signals to selectively enable and disable the contacts to permit selective transmission of the test signals to the wafer contacts.
4. The probe card of claim 3 wherein the semiconductor material comprises silicon and the contacts comprise etched portions of the substrate.

US 6,246,250 B1

13

5. The probe card of claim 3 wherein the contacts comprise a plurality of projections for penetrating the wafer contacts.

6. The probe card of claim 3 wherein the contacts comprise a plurality of test sites, with each of the test sites configured to test a device under test on the wafer.

7. In a test system including a tester for generating test signals, a probe card for applying the test signals to a semiconductor wafer having a plurality of wafer contacts comprising:

a substrate comprising a semiconductor material;

a plurality of contacts comprising raised portions of the substrate and penetrating projections on the raised portions at least partially covered by conductive layers configured to electrically contact the wafer contacts; and

a multiplex circuit comprising a plurality of integrated circuits integral with the substrate in electrical communication with the contacts, the multiplex circuit configured to fan out the test signals to expand resources of the tester;

the integrated circuits comprising a plurality of active electrical switching devices, each of the devices in electrical communication with a contact and operable by control signals to selectively enable and disable the contact, to allow the test signals to be selectively transmitted to a selected wafer contact.

8. The probe card of claim 7 wherein the contacts comprise etched portions of the substrate.

9. The probe card of claim 7 wherein the raised portions comprise surfaces configured to limit a penetration depth of the projections into the wafer contacts.

10. A test system for a semiconductor wafer having a plurality of wafer contacts comprising:

a tester comprising test circuitry for generating test signals and a plurality of electrical paths in electrical communication with the test circuitry, the tester having tester resources determined by a signal generating and analyzing capability and by a number of the electrical paths;

a probe card comprising a substrate comprising a semiconductor material;

a plurality of contacts comprising portions of the substrate at least partially covered with conductive layers configured to make temporary electrical connections with the wafer contacts; and

a multiplex circuit comprising integrated circuits integral with the substrate including a plurality of active electrical switching devices in electrical communication with the tester and with the contacts, the multiplex circuit configured to expand the tester resources by fanning out at least some of the test signals to the contacts while allowing a defective device under test to be electrically disconnected.

11. The probe card of claim 10 wherein the test signals include write signals and the multiplex circuit is configured to fan out and transmit the write signals to a plurality of devices under test on the wafer.

12. The probe card of claim 10 wherein the semiconductor material comprises silicon and the contacts comprise etched portions of the substrate.

14

13. A test system for testing a semiconductor wafer having a plurality of wafer contacts comprising:

a tester configured to transmit test signals to the wafer, the tester comprising test circuitry for generating test signals and a plurality of electrical paths in electrical communication with the test circuitry, the tester having tester resources determined by a signal generating and analyzing capability and by a number of the electrical paths;

a probe card comprising a substrate comprising a semiconductor material;

a plurality of contacts on the substrate in electrical communication with the electrical paths configured to electrically contact the wafer contacts; and

a multiplex circuit comprising a plurality of integrated circuits integral with the substrate including a plurality of active electrical switching devices in electrical communication with the contacts, the circuit configured to fan out the test signals from the tester, and to control the contacts to selectively transmit the test signals to the wafer contacts for expanding the tester resources.

14. The test system of claim 13 wherein the contacts comprise projections for penetrating the wafer contacts.

15. The test system of claim 13 wherein the contacts are at least partially covered with conductive layers.

16. The test system of claim 13 wherein the contacts comprise etched portions of the substrate with projections configured to penetrate the second contacts.

17. A test system for testing a semiconductor wafer having a plurality of wafer contacts comprising:

a tester comprising test circuitry and a plurality of electrical paths configured to transmit write test signals to the wafer and to analyze read test signals from the wafer, the tester having tester resources determined by the test circuitry and the electrical paths;

a probe card comprising a semiconductor substrate and a plurality of contacts on the substrate comprising portions of the substrate at least partially covered by conductive layers in electrical communication with the electrical paths and configured to electrically contact the wafer contacts;

a multiplex circuit on the probe card in electrical communication with the contacts and configured to multiply the test signals for expanding the tester resources;

the multiplex circuit comprising a plurality of integrated circuits integral with the substrate including a plurality of active electrical switching devices, each of the devices in electrical communication with a contact on the probe card and operable by control signals to selectively enable and disable the contact, to allow the test signals to be selectively transmitted to a selected wafer contact.

18. The test system of claim 17 wherein the semiconductor material comprises silicon and the contacts comprise etched portions of the substrate.

19. The test system of claim 17 further comprising a wafer prober and a flexible membrane physically and electrically attaching the probe card to the wafer prober.

* * * * *



US006888366B2

(12) **United States Patent**
Kim et al.

(10) **Patent No.:** US 6,888,366 B2
(45) **Date of Patent:** May 3, 2005

(54) **APPARATUS AND METHOD FOR TESTING
A PLURALITY OF SEMICONDUCTOR
CHIPS**

(75) Inventors: **Hong-Beom Kim**, Suwon (KR); **Ho-Jin Park**, Yongin (KR); **Sung-Hwan In**, Seoul (KR); **Ha-Il Kim**, Seoul (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.** (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/458,437**

(22) Filed: **Jun. 10, 2003**

(65) **Prior Publication Data**

US 2004/0041579 A1 Mar. 4, 2004

(30) **Foreign Application Priority Data**

Aug. 29, 2002 (KR) 10-2002-0051598

(51) Int. Cl.⁷ **G01R 31/26**

(52) U.S. Cl. **324/765; 324/73.1; 714/724**

(58) Field of Search 324/73.1, 754,
324/759, 763-765, 158.1; 714/718, 724,
729, 735-736, 738; 702/118-119

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,675,544 A * 10/1997 Hashimoto 365/201
5,794,175 A * 8/1998 Conner 702/119
6,452,411 B1 * 9/2002 Miller et al. 324/765
6,466,007 B1 * 10/2002 Prazeres da Costa et al. ... 324/
158.1
6,480,978 B1 * 11/2002 Roy et al. 714/724

* cited by examiner

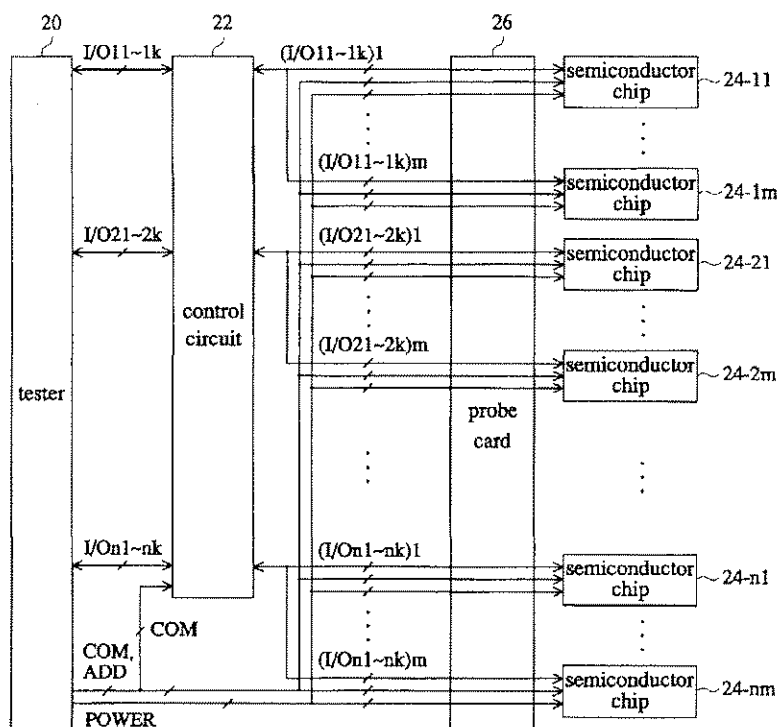
Primary Examiner—Minh N. Tang

(74) Attorney, Agent, or Firm—F. Chau & Associates, LLC

(57) **ABSTRACT**

A semiconductor chip test system and test method thereof are provided. The system having a plurality of data input/output pins, a tester for inputting/outputting data through the plurality of data input/output pins; a plurality of semiconductor chips to be tested by the tester; a control circuit for sequentially outputting the output data from each of the plurality of semiconductor chips to the tester during a read operation and simultaneously supplying the input data from the tester to the semiconductor chips during a write operation.

11 Claims, 11 Drawing Sheets



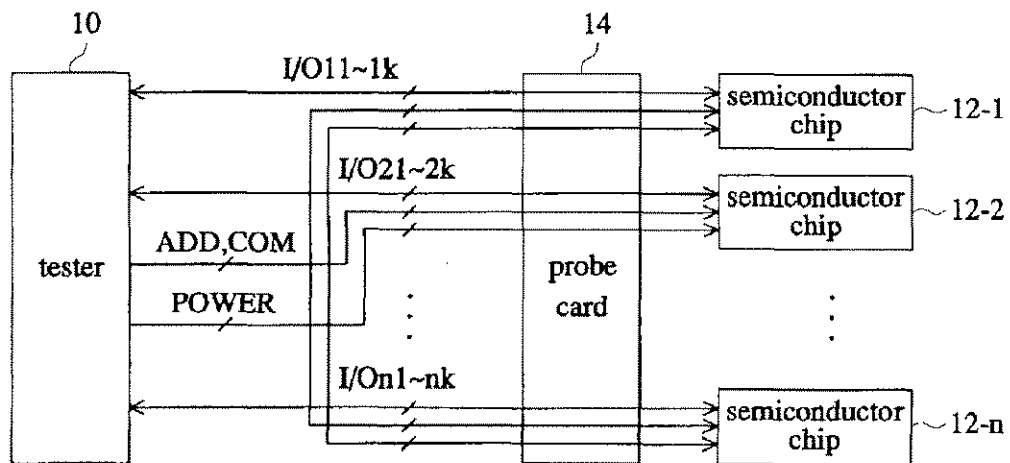
U.S. Patent

May 3, 2005

Sheet 1 of 11

US 6,888,366 B2

FIG. 1
(PRIOR ART)



U.S. Patent

May 3, 2005

Sheet 2 of 11

US 6,888,366 B2

FIG. 2

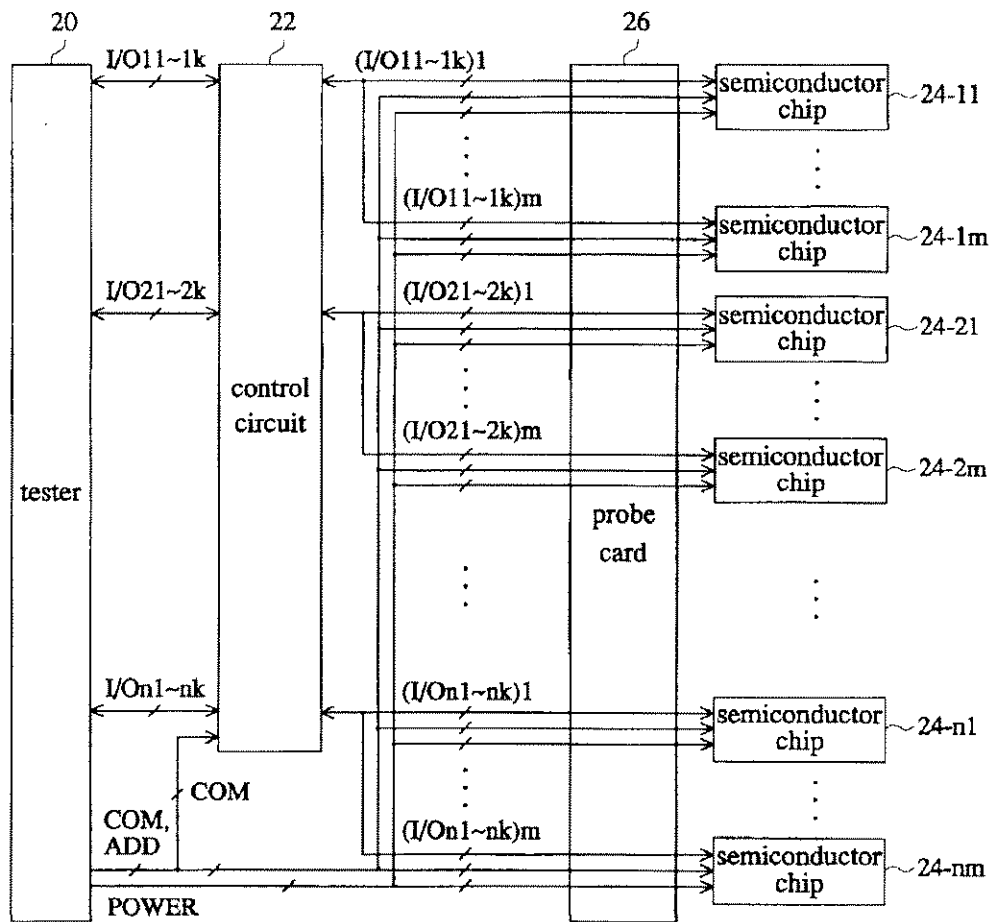


FIG. 3

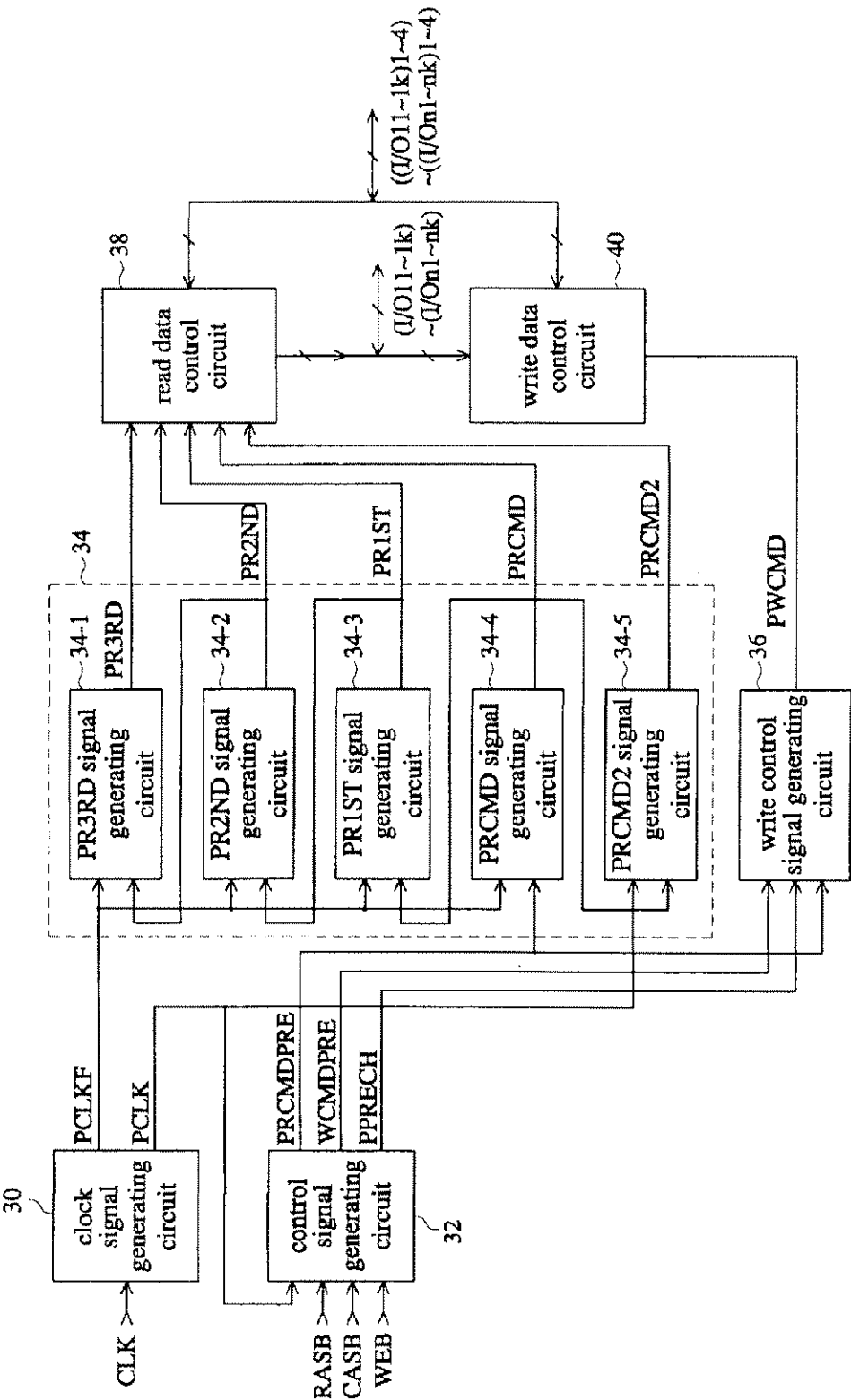


FIG. 4

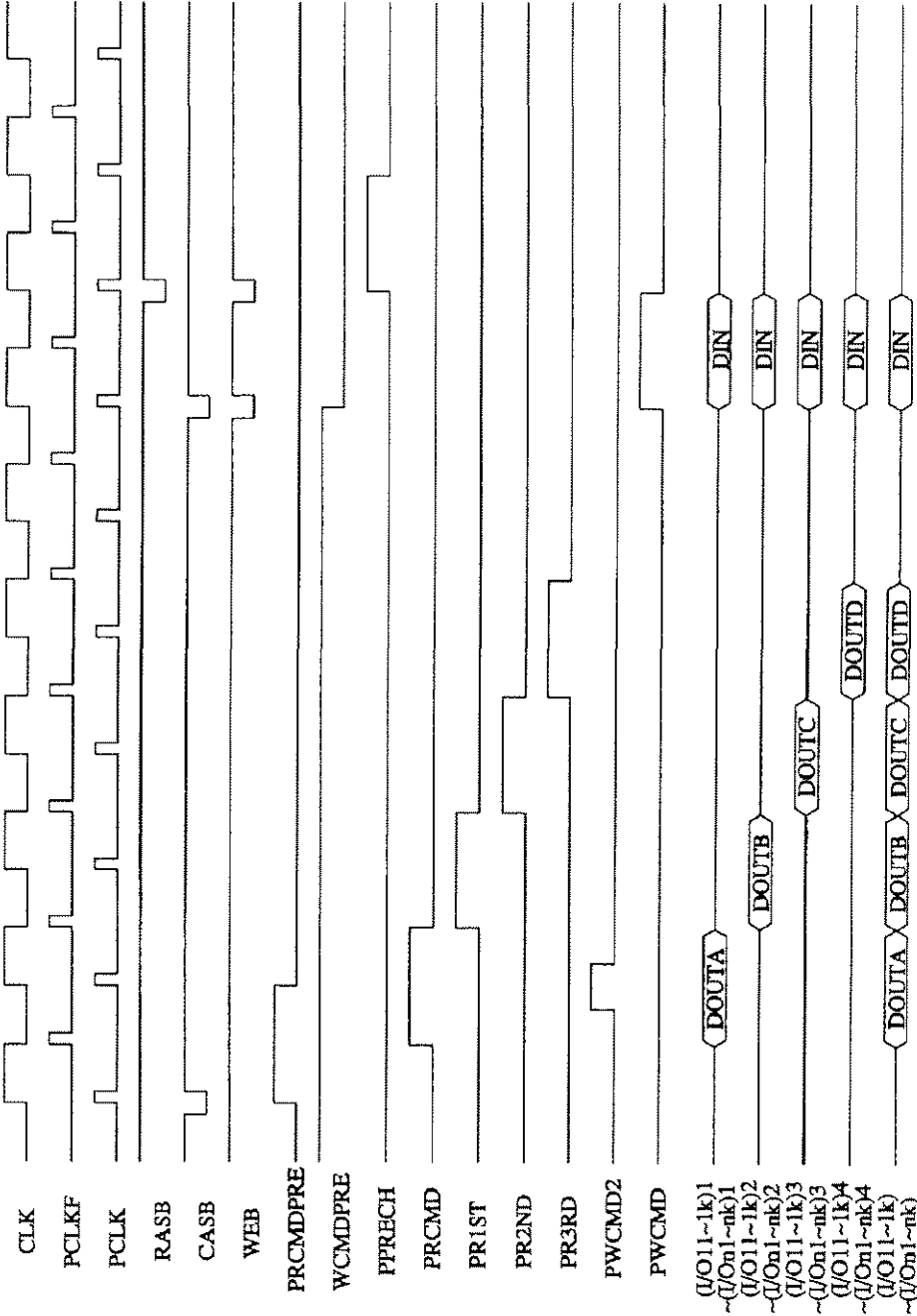


FIG. 5

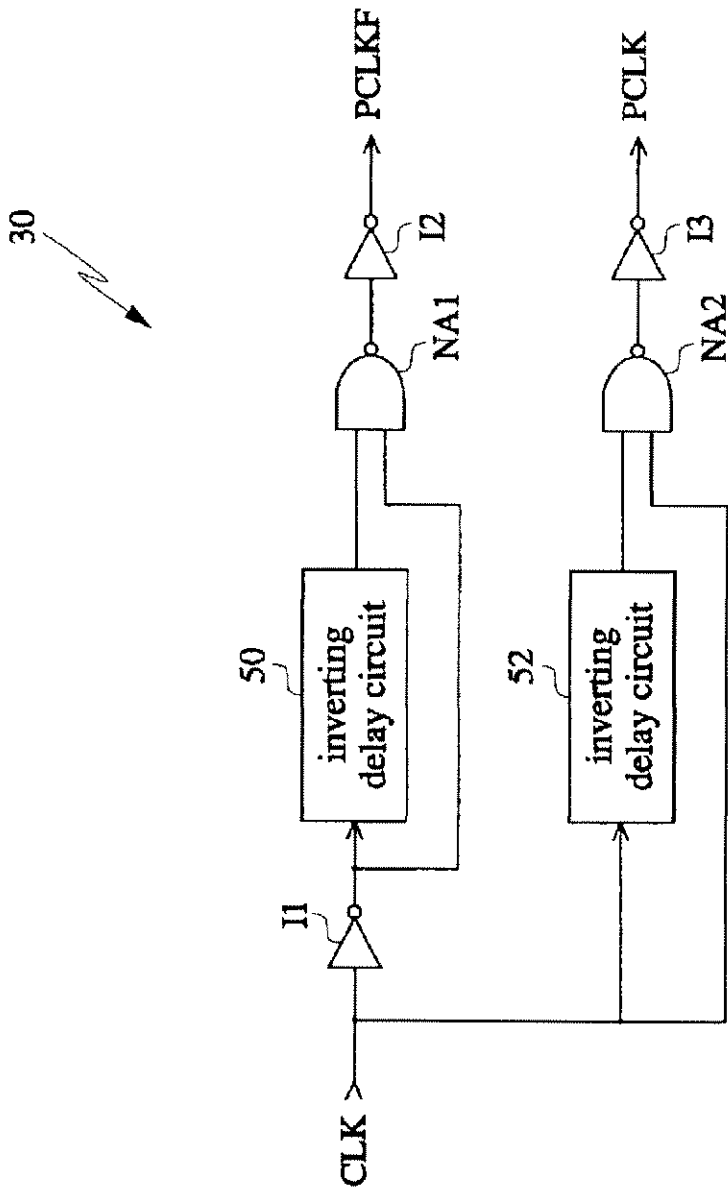


FIG. 6

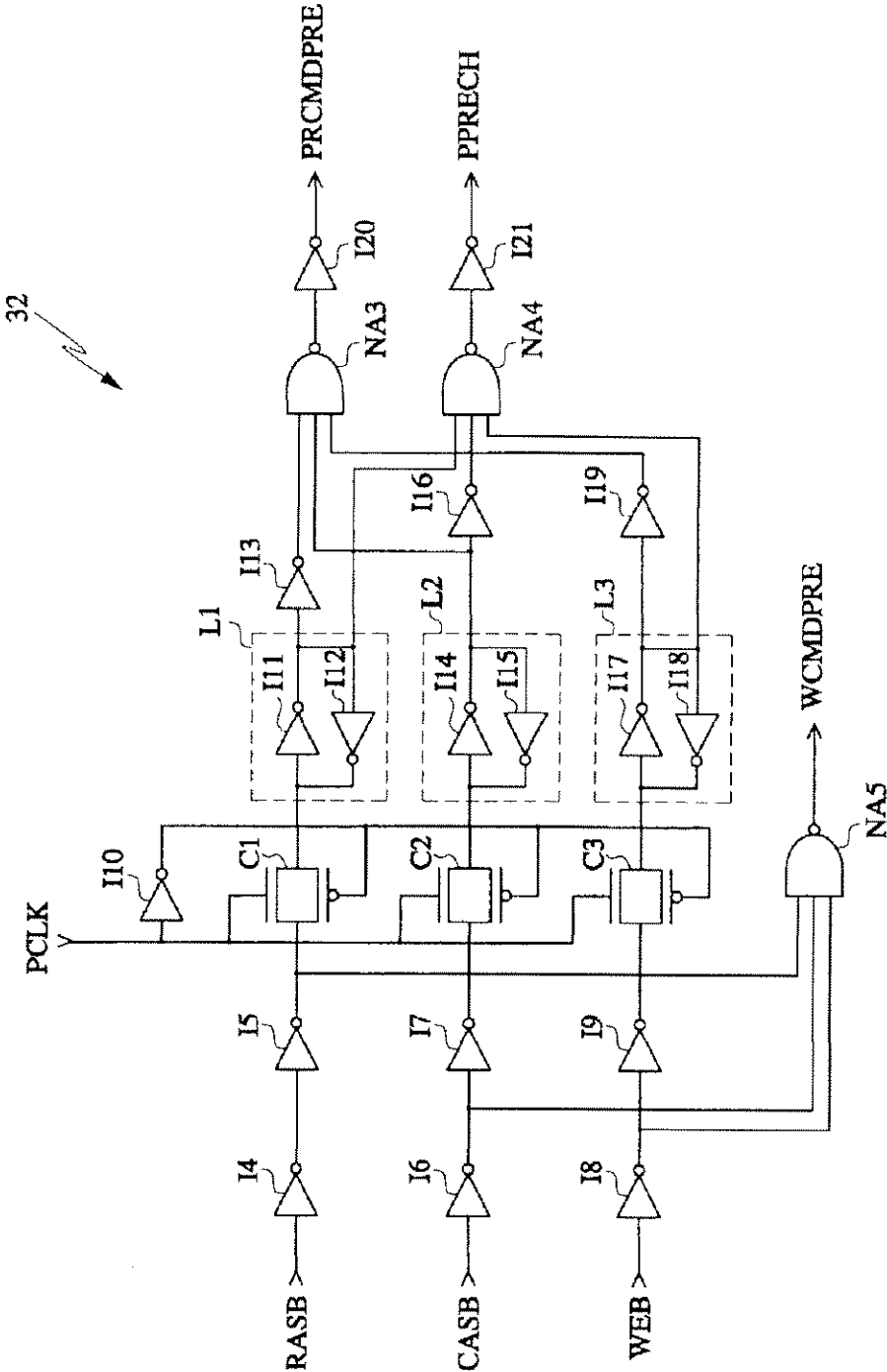


FIG. 7

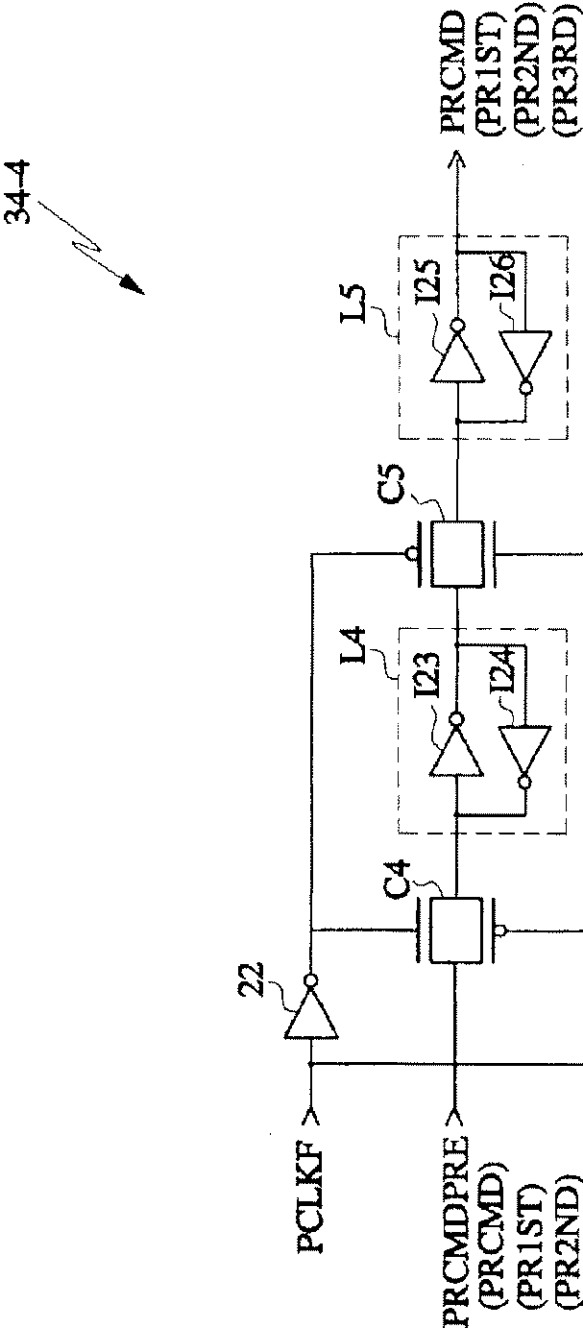


FIG. 8

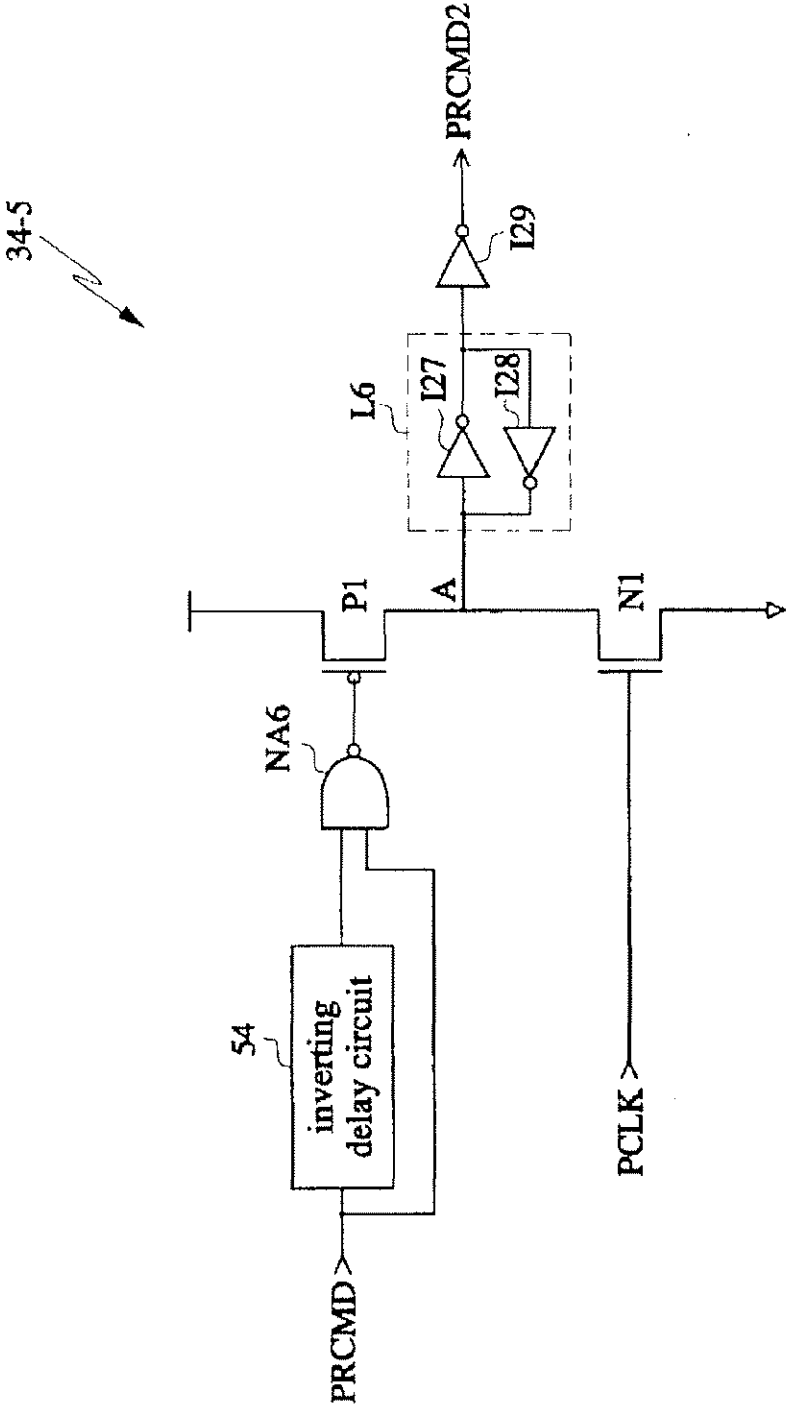


FIG. 9

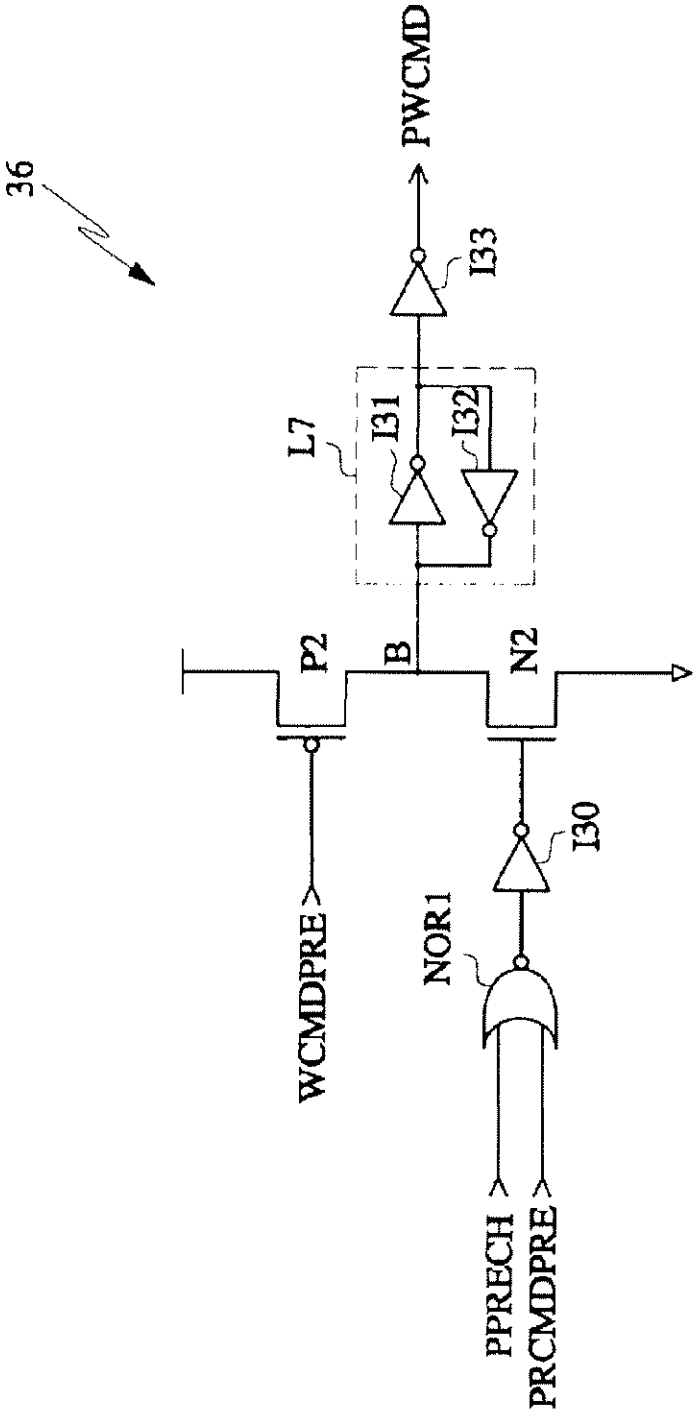


FIG. 10

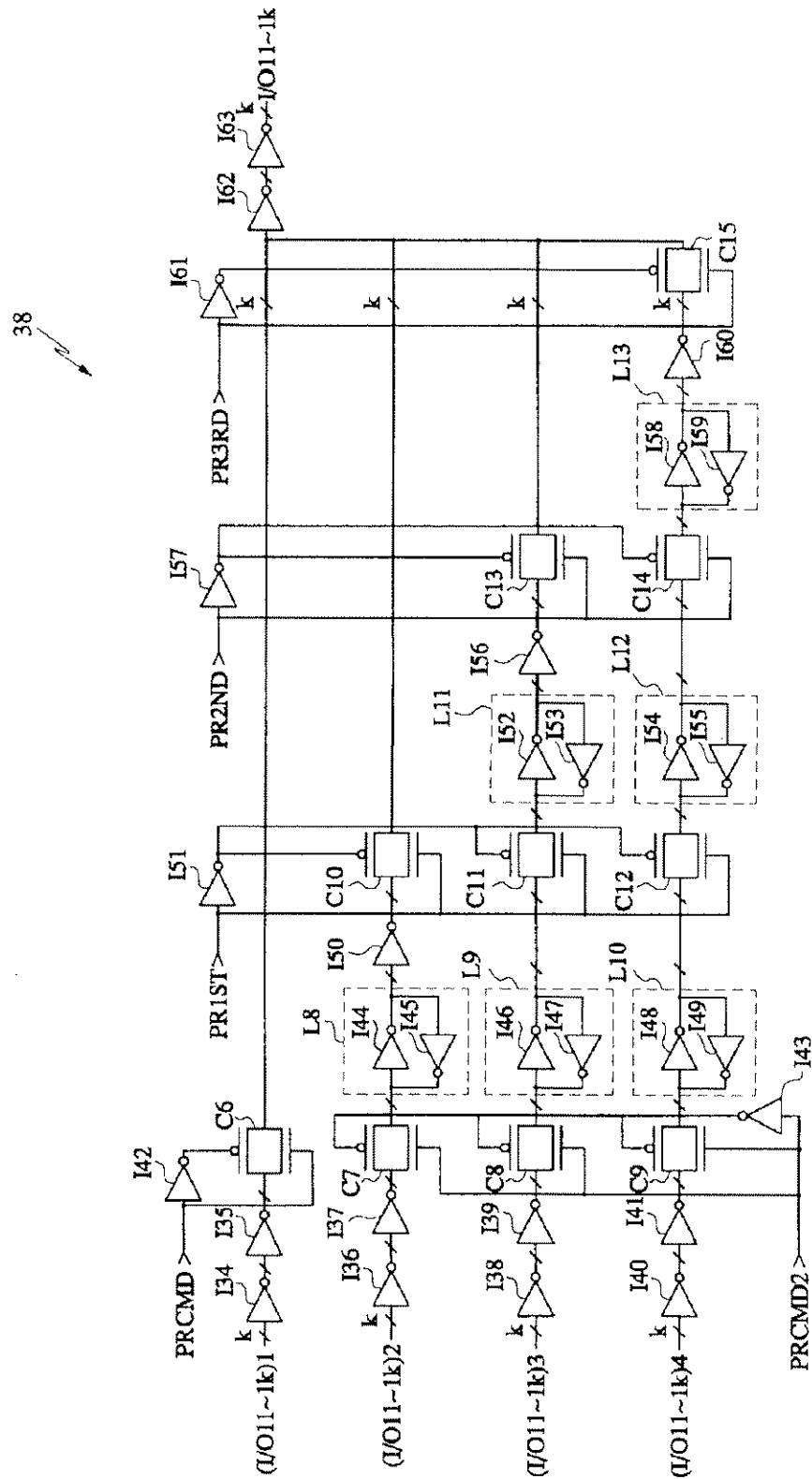
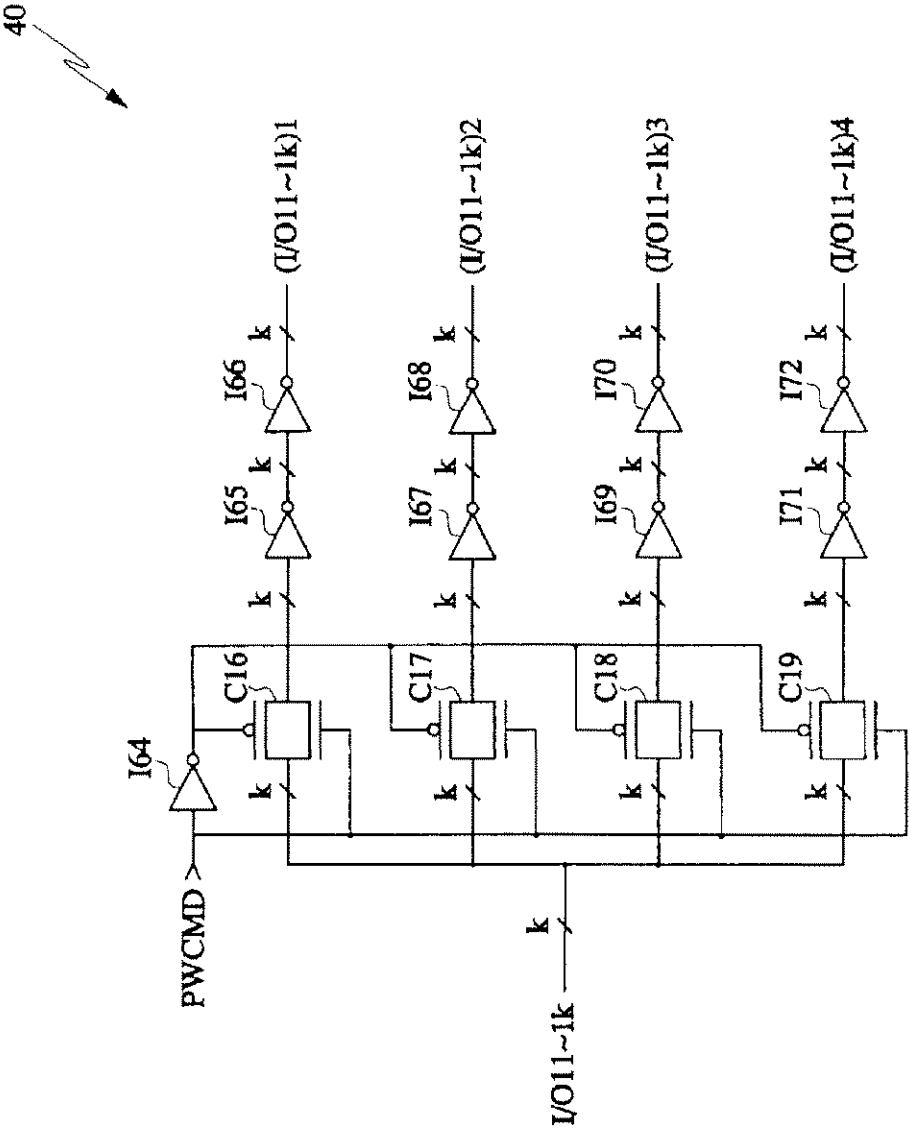


FIG. 11



US 6,888,366 B2

1

APPARATUS AND METHOD FOR TESTING A PLURALITY OF SEMICONDUCTOR CHIPS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a semiconductor chip test system, and more particularly, to a system and method for increasing a number of semiconductor chips to be tested in parallel.

2. Description of Related Art

A conventional semiconductor chip test system includes a tester, a probe card, and semiconductor chips to be tested.

The conventional semiconductor chip test system is limited by the number of the semiconductor chips capable of being tested in parallel. For example, if there are 64 input/output pins on the tester of the semiconductor chip test system, the test system can test only 8 semiconductor chips in parallel each of which have eight (8) input/output pins.

FIG. 1 shows a schematic block diagram of the conventional semiconductor chip test system including the tester 10, semiconductor chips 12-1~12-n, and a probe card 14.

Symbols I/O11~1k, I/O21~2k, . . . , I/On1~nk are indicative of data input/output lines connected between data input/output pads (or, pins) of the semiconductor chips 12-1~12-n and data input/output pins (not shown) of the tester 10. Symbols ADD and COM are indicative of address and command input lines connected between address and command input pins (not shown) of the tester 10 and address and command input pads (or pins) (not shown) of the semiconductor chips 12-1~12-n. A symbol POWER is indicative of power supplying lines connected between power supply pins (not shown) of the tester 10 and power supplying pads (or pins) of the semiconductor chips 12-1~12-n.

The tester 10 inputs/outputs data from/to the semiconductor chips 12-1~12-n comprising k data input/output pads (or pins) through the data input/output lines I/O11~1k . . . I/On1~nk, outputs the address and the command to the semiconductor chips 12-1~12-n through the address and command output lines ADD and COM, and applies the power supply through the power supplying lines POWER. At this time, the data are transferred between the tester 10 and the semiconductor chips 12-1~12-n through the probe card 14. Also, the address, the command, and the power supply are applied from the tester 10 to the semiconductor chips 12-1~12-n through the probe card 14. When the semiconductor chips are tested at a wafer level, the tester 10 is connected to the data input/output pads of the chips. When the semiconductor chips are tested at a package level, the tester 10 is connected to the data input/output pins of the chips.

In the test system described above, there is no problem in that the address and the command output lines ADD and COM, and the power supplying lines POWER are commonly connected from the tester 10 to the n semiconductor chips 12-1~12-n. In other words, the tester 10 outputs a signal through the address and command output lines ADD and COM, and the power supplying lines POWER. The signal lines are configured to be in n groups and being connected to each of n semiconductor chips 12-1~12-n through the probe card 14.

However, n groups of the data input/output lines ((I/O11~I/O1k)~(I/On1~I/Onk)) of the tester 10 are not com-

2

monly connected to n semiconductor chips 12-1~12-n but are connected to each of n semiconductor chips 12-1~12-n, since data which is written from the tester to the semiconductor chips is same, but data which is read from the semiconductor chips to the tester can be different.

Accordingly, the conventional semiconductor chip test system can not commonly use the data input/output lines, and thus, if the number of the data input/output pads (or pins) of each of n semiconductor chips 12-1~12-n is k, the conventional semiconductor test system has to input/output the data through nk data input/output lines. As a result, the number of the semiconductor chips to be tested are limited to the number of the data input/output pins of the tester of the semiconductor chip test system.

SUMMARY OF THE INVENTION

A semiconductor chip test system capable of testing semiconductor chips even when the number of data input/output pads (or pins) of semiconductor chips to be tested is higher than a number of a data input/output pins of the tester of the semiconductor chip test system is provided.

According to one aspect of the present invention, a semiconductor chip test system comprises a tester having a plurality of data input/output pins for inputting/outputting data through the plurality of data input/output pins, a plurality of semiconductor chips to be tested by the tester, and a control circuit for sequentially outputting the data output from each of the plurality of semiconductor chips to the tester during a read operation and supplying the data input from the tester to the plurality of semiconductor chips during a write operation.

According to another aspect of the present invention, a semiconductor chip test system comprises a tester having n groups of data input/output pins of which each of the groups include k data input/output pins for inputting/outputting data through the plurality of data input/output pins, n groups of semiconductor chips, each group including m semiconductor chips, each semiconductor chip comprising k data input/output pads (or pins) to be tested by the tester, and a control means for sequentially outputting the data input from a first one to m_n one of each of the n groups of semiconductor chips to the tester during a read operation and simultaneously supplying nk data output from the tester to the n groups of semiconductor chips during a write operation.

The control means comprises a clock signal generating means for generating a first clock signal in response to a rising edge of a clock signal input from the tester and generating a second clock signal in response to a falling edge of the clock signal input from the tester, a control signal generating means for generating a read command and a write command by inputting a command input from the tester, a read control signal generating means for sequentially generating m read control signals by inputting the read command in response to the second clock signal, a write control signal generating means for generating a write control signal in response to the write command, a read data control means for sequentially outputting the output data from a first semiconductor chip to the m_n semiconductor chip of each of the n groups of semiconductor chips to the tester in response to the m read control signals, and a write data control means for simultaneously outputting the data input from the tester to the n groups of semiconductor chips in response to the write control signal.

According to a further aspect of the present invention, a test method of the semiconductor chip test system is provided, the system including a tester having n groups of

US 6,888,366 B2

3

data input/output pins of which each of the groups include k data input/output pins for inputting/outputting data through the data input/output pins, and n groups of semiconductor chips being respectively including m semiconductor chips, and each of the m semiconductor chips comprising k data input/output pads (or pins) to be tested by the tester, comprises steps of sequentially outputting the input data from a first semiconductor chip to m_{th} semiconductor chip for each of the n groups of the semiconductor chips to the tester during a read operation and simultaneously supplying nk data output from the tester to the n groups of semiconductor chips during a write operation.

According to another aspect, the test method further comprises steps of generating a first clock signal in response to a rising edge of a clock signal input from the tester, generating a second clock signal in response to a falling edge of the clock signal from the tester, and generating a read command and a write command by inputting a command input from the tester, generating sequentially m read control signals by inputting the read command in response to the second clock signal, and generating a write control signal in response to the write command, and outputting sequentially output data from the first semiconductor chip to the m_{th} semiconductor chip for each of the n groups of semiconductor chips to the tester in response to each of the m read control signals during the read operation and simultaneously outputting the data input from the tester to the n groups of semiconductor chips in response to the write control signal during the write operation.

Other aspects, features and advantages of the present invention are disclosed in a detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, in which like reference numerals designate like elements, and in which:

FIG. 1 shows a schematic block diagram of a conventional semiconductor chip test system;

FIG. 2 is a block diagram illustrating an embodiment of a semiconductor chip test system in accordance with the present invention;

FIG. 3 is a block diagram illustrating an embodiment of a control circuit of the semiconductor chip test system of FIG. 2;

FIG. 4 is a timing chart for illustrating an operation of the control circuit of FIG. 3;

FIG. 5 is a circuit configuration of an embodiment of a clock signal generating circuit of FIG. 3;

FIG. 6 is a circuit configuration of an embodiment of a control signal generating circuit of FIG. 3;

FIG. 7 is a circuit configuration of an embodiment of a signal generating circuit of a read control signal generating circuit of FIG. 3.

FIG. 8 is a circuit configuration of an embodiment of a signal generating circuit of the read control signal generating circuit of FIG. 3.

FIG. 9 is a circuit configuration of an embodiment of a write control signal generating circuit of FIG. 3;

FIG. 10 is a circuit configuration of an embodiment of a read data control circuit of FIG. 3; and

FIG. 11 is a circuit configuration of an embodiment of a write data control circuit of FIG. 3.

4

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of a semiconductor test system and method for testing the same according to the present invention will now be described with reference to the accompanying drawings.

FIG. 2 is a block diagram illustrating an embodiment of a semiconductor chip test system in accordance with the present invention.

Referring to FIG. 2, the semiconductor chip test system of the present invention comprises a tester 20, a control circuit 22, a plurality of a semiconductor chips ((24-11~24-2m)~(24-n1~24-2nm)), and a probe card 26.

Symbols I/O11~I/O1k, I/O21~I/O2k, I/On1~I/Onk are indicative of data input/output lines connected between data input/output pins (not shown) of the tester 20 and the control circuit 22. Symbols ((I/O11~I/k) 1~m, (I/O21~2k) 1~m, . . . , (I/On1~nk) 1~m) are indicative of data input/output lines connected between the control circuit 22 and data input/output pads (or pins) of the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)) respectively. Symbols ADD and COM are indicative of address and command input lines connected between address and command input pins (not shown) of the tester 20 and address and command input pads (or pins) (not shown) of the control circuit 22 or the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)). A symbol POWER is indicative of power supply lines connected between power supplying pins (not shown) of the tester 20 and power supply input pads (or pins) (not shown) of the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)).

The tester 20 includes k data input/output pins (not shown) similar to those of the tester 10 shown in FIG. 1. The tester 20 inputs/outputs data through the data input/output lines I/O11~I/O1k, I/O21~I/O2k . . . I/On1~I/Onk and supplies the address, the command and the power supply to the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)) through the address and command output lines ADD and COM, and the power supply lines POWER.

The control circuit 22 inputs a command input through the command output lines COM and extends data input through n groups of k data input/output lines I/O11~I/O1k, I/O21~I/O2k . . . I/On1~I/Onk by m during a write operation. The extended data are applied to the n groups of the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)) having k data input/output pads (or pins) through the n groups of m data input/output lines each having k data input/output lines ((I/O11~I/O1k) 1~m, . . . , (I/On1~I/Onk) 1~m). Also, the control circuit 22 inputs a command input through the command output lines COM and inputs all of k data output from each of n groups of the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)) having k data input/output pads (or pins) during a read operation, and then sequentially outputs the data output from the first semiconductor chips (24-11~24-1m) to the m_{th} semiconductor chips (24-n1~24-nm) of n groups of the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)) through n groups of k data input/output lines ((I/O11~I/O1k)1~(I/On1 I/Onk)m) to the tester 20. In other words, the control circuit 22 extends the n groups of k data output from the tester 20 by m and simultaneously writes the extended data to the n groups of the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)) during the write operation. Also, the control circuit 22 simultaneously inputs k data

US 6,888,366 B2

5

output from each of n groups of the semiconductor chips ((24-11~24-1m), (24-21~24-2m), . . . (24-n1~24-nm)) during the read operation, and then sequentially outputs k data output from the first semiconductor chip (24-11~24-n1) to the m_{th} semiconductor chip (24-1m~24-nm) of each of n groups of the semiconductor chips ((24-11~24-1m)~(24-n1~24-nm)) through n groups of k data input/output lines ((I/O11~1k)~(I/On1~nk)) to the tester 20. The data transfer between the control circuit 22 and the n groups of the semiconductor chips ((24-11~24-1m)~(24-n1~24-nm)) is performed through the probe card 26.

Consequently, an embodiment of semiconductor chip test system of the present invention of FIG. 2 can simultaneously test nm number of semiconductor chips having k data input/output pads (or pins) using the tester 20, wherein the number of the data input/output pins is nk .

FIG. 3 is a block diagram of an embodiment of a control circuit of the semiconductor chip test system of FIG. 2. The control circuit includes a clock signal generating circuit 30, a control signal generating circuit 32, a read control signal generating circuit 34, a write control signal generating circuit 36, a read data control circuit 38, and a write data control circuit 40.

The read control signal generating circuit 34 includes a PR3RD signal generating circuit 34-1, a PR2ND signal generating circuit 34-2, a PR1ST signal generating circuit 34-3, a PRCMD signal generating circuit 34-4 and a PRCMD2 signal generating circuit 34-5.

The control circuit of the semiconductor chip test system of FIG. 3 inputs/outputs the input and output data through nk data input/output lines ((I/O11~1k)~(I/On1~nk)) over the data input/output lines (((I/O11~1k)1~4)~((I/On1~nk)1~4)).

Now, it will be explained in detailed to the operation for each of the blocks of FIG. 3 will be explained in detail.

The lock signal generating circuit 30 generates a clock signal PCLKF and PCLK in response to a clock signal CLK. The control signal generating circuit 32 inputs the clock signal PCLK, an inverted low address strobe signal RASB, a n inverted column address strobe signal CASB, and an inverted write enable signal WEB, to generate a read command PRCMDPRE, a write command WCMDPRE, and a precharge command PPRECH. The read control signal generating circuit 34 inputs the clock signal PCLKR and a read command PRCMDPRE to generate the read control signals PRCMD, PR1ST, PR2ND and PR3RD, and inputs the clock signal PCLK and the read control signal PRCMD to generate a latch timing control signal PRCMD2. The read control signals PRCMD, PR1ST, PR2ND and PR3RD are sequentially generated by being delayed by one clock cycle in response to the clock signal PCLK. The write control signal generating circuit 36 inputs the read command PRCMDPRE, the write command WCMDPRE, and the precharge command PPRECH to generate the write control signal PWCMD. The write data control circuit 40 extends data input from the data input/output lines ((I/O11~1k)~(I/On1~nk)) 4 times in response to the write control signal PWCMD and simultaneously outputs the extended data to the data input/output lines (((I/O11~1k)1~4)~((I/On1~nk)1~4)), during the write operation. The read data control circuit 38 simultaneously inputs the data input from the data input/output lines (((I/O11~1k)1~4)~((I/On1~nk)1~4)) and sequentially outputs the data input from the data input/output lines (((I/O11~1k)1~4)~((I/On1~nk)1~4)) to the data input/output lines ((I/O11~1k)~(I/On1~nk)) in response to the read control signals PRCMD, PR1ST, PR2ND and PR3RD, and the latch timing control signal PRCMD2.

6

FIG. 4 is a timing chart for illustrating the operation of the control circuit of FIG. 3. The clock signal generating circuit 30 generates the clock signal PCLK by detecting a rising edge of the clock signal CLK, and generates the clock signal PCLKF by detecting a falling edge of the clock signal CLK.

Firstly, the operation for reading a test data will be explained.

When the inverted low address strobe signal RASB and the inverted write enable signal WEB of high level, and the inverted column address strobe signal CASB of low level are supplied to the control signal generating circuit 32, the control signal generating circuit 32 generates a read command PRCMDPRE in response to the clock signal PCLK.

When the read command PRCMDPRE is generated from the control signal generating circuit 32, the read control signal generating circuit 34 generates the read control signal PRCMD in response to the clock signal PCLKF, and generates the read control signals PR1ST, PR2ND and PR3RD by sequentially delaying the read control signal PRCMD in response to the clock signal PCLKF by the one clock cycle. Also, the read control signal generating circuit 34 generates the latch timing control signal PRCMD2 in response to the read control signal PRCMD and the clock signal PCLK. At this time, the generated signal PRCMD2 is used as a signal for correctly latching the data input through the data input/output lines (((I/O11~1k)1~4)~((I/On1~nk)1~4)).

The read data control circuit 38 outputs the data DOUTA input from the data input/output lines ((I/O11~1k)1~(I/On1~nk)1) to the data input/output lines ((I/O11~1k)~(I/On1~nk)) in response to the read control signal PRCMD. The read data control circuit 38 also latches data DOUTB, DOUTC, DOUTD input from the data input/output lines ((I/O11~1k)2~(I/On1~nk)4) in response to the latch timing control signal PRCMD2, outputs to the data input/output lines ((I/O11~1k)~(I/On1~nk)) the data DOUTB input from the data input/output lines ((I/O11~1k)2~(I/On1~nk)2) in response to the read control signal PR1ST, outputs to the data input/output lines ((I/O11~1k)~(I/On1~nk)) the data DOUTC input from the data input/output lines ((I/O11~1k)3~(I/On1~nk)3) in response to the read control signal PR2ND, and outputs to the data input/output lines ((I/O11~1k)~(I/On1~nk)) the data DOUTD input from the data input/output lines ((I/O11~1k)4~(I/On1~nk)4) in response to the read control signal PR3RD.

Next, the operation for writing the test data will be explained.

When the inverted low address strobe signal RASB of high level, the inverted write enable signal WEB and the inverted column address strobe signal CASB of low level are supplied to the control signal generating circuit 32, the control signal generating circuit 32 generates a write command WCMDPRE.

The write control signal generating circuit 36 generates the write control signal PWCMD in response to the write command WCMDPRE. Also, the write data control circuit 40 simultaneously outputs the data DIN input from the data input/output lines ((I/O11~1k)~(I/On1~nk)) to the data input/output lines ((I/O11~1k)1~4)~((I/On1~nk)1~4) in response to the write control signal PWCMD.

Next, when the inverted low address strobe signal RASB and the inverted write enable signal of low level, and the inverted column address strobe signal CASB of high level are supplied to the control signal generating circuit 32, the control signal generating circuit 32 generates the precharge command PPRECH.

When the precharge command PPRECH is generated by the control signal generating circuit 32, the write control signal generating circuit 36 disables the write control signal PWCMD.

US 6,888,366 B2

7

FIG. 5 is a circuit configuration of an embodiment of the clock signal generating circuit 30 of FIG. 3. The clock signal generating circuit 30 is constituted of a clock signal PCLKF generating circuit including an inverting delay circuit 50, NAND gate NA1, and an inverters I1 and I2, and a clock signal PCLK generating circuit including an inverting delay circuit 52, a NAND gate NA2, and an inverter I3.

Next, the operation for each of the elements of the clock signal generating circuit 30 of FIG. 5 will be explained.

The inverter I1 inverts the clock signal CLK. The inverting delay circuit 50 inverts and delays an output signal of the inverter I1. The NAND gate NA1 NANDs the output signals of both the inverter I1 and the inverting delay circuit 50. The inverter I2 inverts the output signal of the NAND gate NA1 to generate the clock signal PCLKF. The inverting delay circuit 52 inverts and delays the clock signal CLK. The NAND gate NA2 NANDs the output signal of the inverting delay circuit 52 and the clock signal CLK. The inverter I3 inverts the output signal of the NAND gate NA2 to generate the clock signal PCLK.

The clock signal generating circuit 30 shown in FIG. 5 generates the clock signal PCLKF in response to the falling edge of the clock signal CLK. At this time, the generated clock signal PCLKF has a pulse width of the delayed time of the inverting delay circuit 50. Also, the clock signal generating circuit generates the clock signal PCLK in response to the rising edge of the clock signal CLK. At this time, the generated clock signal PCLK has a pulse width of the delayed time of the inverting delay circuit 52.

FIG. 6 is a circuit configuration of an embodiment of the control signal generating circuit 32 of FIG. 3. The control signal generating circuit 32 includes inverters I4-I21, CMOS transfer gates C1, C2 and C3, and NAND gates NA3, NA4, and NA5.

Referring to FIG. 6, the inverters I11 and I12 compose latch L1, the inverters I14 and I15 compose latch L2, and the inverters I17 and I18 compose latch L3.

Next, the operation of the elements shown in FIG. 6 will be explained.

The inverters I4 and I5 perform a buffering operation for the inverted low address strobe signal RASB. The inverters I6 and I7 perform the buffering operation for the inverted column address strobe signal CASB. The inverters I8 and I9 perform the buffering operation for the inverted write enable signal WEB. When the CMOS transfer gates C1, C2 and C3 are turned on in response to the clock signal PCLK of high level, the CMOS transfer gates transfer the output signals of the inverter I5, I7 and I9. The latches L1, L2 and L3 invert and latch the output signals of the CMOS transfer gates C1, C2 and C3. The inverters I11, I14 and I17 invert the output signals of the latch L1, L2 and L3 respectively. The NAND gate NA3 NANDs the output signal of the inverter I13, the output signal of the latch L2 and the output signal of the inverter I19. The inverter I20 inverts the output signal of the NAND gate NA3 to generate the read command PRCMDPRE. The NAND gate NA4 NANDs the output signal of the latch L1, the output signal of the inverter I16 and the output signal of the latch L3. The inverter I21 inverts the output signal of the NAND gate NA4 to generate the precharge command PPRECH. The NAND gate NA5 NANDs the output signals of the inverter I5, I6, and I8 to generate the write command WCMDPRE.

That is, the control signal generating circuit 32 shown in FIG. 6, in response to the clock signal PCLK of high level, and latches the inverted low address strobe signal RASB, the inverted write enable signal WEB and the inverted column

8

address strobe signal CASB by the latches L1, L2 and L3. At this time, when the signals latched by the latches L1, L2 and L3 are respectively at high level, low level and high level, the control signal generating circuit generates the read command PRCMDPRE. Also, when the signals latched by the latches L1, L2, and L3 are at low level, high level and low level, the control signal generating circuit generates the precharge command PPRECH. When the inverted low address strobe signal RASB of high level, the inverted write enable signal WEB and the inverted column address strobe signal CASB of low level, regardless of the state of the clock signal PCLK, are applied to the control signal generating circuit, the control signal generating circuit generates a write command WCMDPRE of high level.

FIG. 7 is a circuit configuration of an embodiment of a PRCMD signal generating circuit 34-4 of the read control signal generating circuit shown in FIG. 3. The PRCMD signal generating circuit includes CMOS transfer gates C4 and C5, and inverters I22-I26.

Referring to FIG. 7, the inverters I23 and I24 compose the latch L4, and the inverters I25 and I26 compose the latch L5.

Next, the operation for the elements shown in FIG. 7 will be explained.

The CMOS transfer gate C4 transfers the read command PRCMDPRE in response to the clock signal PCLKF of high level. The latch L4 inverts and latches the output signal of the CMOS transfer gate C4. The CMOS transfer gate C5 transfers the output signal of the latch L4 in response to the clock signal PCLKF of high level. The latch L5 inverts and latches the output signal of the CMOS transfer gate C5 to generate the signal PRCMD.

The PRCMD signal generating circuit 34-4 shown in FIG. 7 latches the read command PRCMDPRE in response to the clock signal PCLKF of low level, and latches the latched signal in response to the clock signal PCLKF of high level, thereby generating the signal PRCMD.

PR1ST, PR2ND and PR3RD signal generating circuits are of the same configuration as the PRCMD signal generating circuit shown in FIG. 7.

In other words, the read control signal generating circuit delays the read command PRCMDPRE in response to the clock signal PCLKF to generate the read control signal PRCMD, delays the read control signal PRCMD by one clock cycle to generate the read control signal PR2ND, and delays the read control signal PR2ND by one clock cycle to generate the read control signal PR3RD.

FIG. 8 is a circuit configuration of an embodiment of the PRCMD2 signal generating circuit 34-5 of the read control signal generating circuit 34 shown in FIG. 3. The PRCMD2 signal generating circuit 34-5 includes inverting delay circuit 54, NAND gate NA6, PMOS transistor P1, NMOS transistor N1, and inverters I27, I28 and I29.

Referring to FIG. 8, the inverters I27 and I28 compose latch L6.

Next, the operation for the elements shown in FIG. 8 will be explained.

The inverting delay circuit 54 inverts and delays the read control signal PRCMD. The NAND gate NA6 NANDs the output signal of the inverting delay circuit 54 and the read control signal PRCMD. The PMOS transistor P1 makes the node A transition to high level in response to the output signal of the NAND gate NA6 of low level. The NMOS transistor N1 makes the node A transition to low level in response to the clock signal PCLK of high level. The latch L6 inverts and latches the signal of the node A. The inverter

US 6,888,366 B2

9

129 inverts the output signal of the latch L6 to generate the latch timing control signal PRCMD2.

The PRCMD2 signal generating circuit shown in FIG. 8 generates the latch timing control signal PRCMD2 transitioning to high level in response to a rising edge of the read control signal PRCMD and transitioning to low level in response to the clock signal PCLK of high level.

FIG. 9 is a circuit configuration of an embodiment of the write control signal generating circuit 36 of FIG. 3. The write control signal generating circuit 36 includes the NOR gate NOR1, inverters I30, I31, I32 and I33, the PMOS transistor P2, and the NMOS transistor N2.

Referring to FIG. 9, the inverters I31, I32 compose latch L7.

Next, the operation for the elements shown in FIG. 9 will be explained.

The NOR gate NOR1 NORs the precharge command PPRECH and the read command PRCHMDPRE. The inverter I30 inverts the output signal of the NOR gate NOR1. A circuit constituted of the NOR gate NOR1 and the inverter I30 generates a high level signal, when the precharge command PPRECH of high level or the read command PRCHMDPRE of high level are input to the circuit. The PMOS transistor P2 is turned on in response to the write command WCMDPRE of low level, and makes the node B transition to high level. The NMOS transistor N2 is turned on in response to the output signal of the inverter I30 of high level, and makes the node B transition to low level. The latch L7 inverts and latches the signal of the node B. The inverter I33 inverts the output signal of the latch L7 to generate the write control signal PWCMD.

When the precharge command PPRECH or the read command PRCHMDPRE of high level are supplied to the write control signal generating circuit 36, the write control signal generating circuit 36 generates the write control signal PWCMD of low level. Also, when the write command WCMDPRE of low level is supplied to the write control signal generating circuit 36, the write control signal generating circuit 36 generates the write control signal PWCMD of high level.

FIG. 10 is a circuit configuration of an embodiment of the read data control circuit 38 of FIG. 3. The read data control circuit includes inverters I34~I63, and CMOS transfer gates C6~C15.

Referring to FIG. 10, the inverters I44 and I45 compose latch L8. The inverters I46 and I47 compose latch L9. The inverters I48 and I49 compose latch L10. Also, the inverters I52 and I53 compose latch L11, the inverters I54 and I55 compose latch L12, and the inverters I58 and I59 compose latch L13.

FIG. 10 shows a circuit for outputting the data input from the data input/output lines ((I/O11~1k)1~4) through the data input/output lines (I/O11~1k). A circuit (not shown) for outputting the data input from the data input/output lines ((I/O21~2k)1~4)~((I/On1~nk)1~4) through the data input/output lines ((I/O21~2k)1~4)~((I/On1~nk)1~4) is of the same configuration as that of FIG. 10.

Next, the operation for the elements of FIG. 10 will be explained.

The inverters (I34, I35), (I36, I37), (I38, I39), and (I40, I41) buffer the data input through each of k data input/output lines (I/O11~1k)1~4. The CMOS transfer gate C6 transfers the output signal of the inverter I35 in response to the read control signal PRCMD of high level. The CMOS transfer gates C7, C8 and C9 respectively transfer the output signals

10

of the inverters I37, I39 and I41 in response to the latch timing control signal PRCMD2 of high level. The latches L8, L9 and L10 respectively invert and latch the output signals of the CMOS transfer gates C7, C8 and C9. The inverter I50 inverts the output signal of the latch L8. The CMOS transfer gates C10, C11 and C12 respectively transfer the output signals of the inverter I50 and the latches L9 and L10 in response to the read control signal PR1ST of high level. The latches L11 and L12 respectively invert and latch the output signals of the CMOS transfer gates C11 and C12. The inverter I56 inverts the output signal of the latch L11. The CMOS transfer gates C13 and C14 respectively transfer the output signals of the inverter I56 and the latch L12 in response to the read control signal PR2ND of high level. The latch L13 inverts and latches the output signal of the CMOS transfer gate C14. The inverter I60 inverts the output signal of the latch L13. The CMOS transfer gate C15 transfers the output signal of the inverter I58 in response to the read control signal PR3RD of high level. The inverters I62 and I63 respectively perform a buffering operation for the signal output from the CMOS transfer gates C6, C10, C13 and transfer the buffered signal to the data input/output lines I/O11~1k.

In other words, the read data control circuit 38 shown in FIG. 10 transfers the data transferred from the data input/output lines ((I/O11~1k)1)) to the data input/output lines (I/O11~1k) in response to the read control signal PRCMD, latches the data transferred from the data input/output lines ((I/O11~1k)2)) in response to the latch timing control signal PRCMD2, and transfers the latched data to the data input/output lines (I/O11~1k) in response to the read control signal PR1ST. Accordingly, the data transferred from the data input/output lines ((I/O11~1k)2)) is transferred to the data input/output lines (I/O11~1k) one clock cycle later after the data transferred from the data input/output lines ((I/O11~1k)1)) is transferred to the data input/output lines (I/O11~1k). Also, the data transferred from the data input/output lines ((I/O11~1k)3)) is transferred to the data input/output lines (I/O11~1k) one clock cycle after the data transferred from the data input/output lines ((I/O11~1k)2)) is transferred to the data input/output lines (I/O11~1k). Similarly, the data transferred from the data input/output lines ((I/O11~1k)4)) is transferred to the data input/output lines (I/O11~1k) one clock cycle after the data transferred from the data input/output lines ((I/O11~1k)3)) is transferred to the data input/output lines (I/O11~1k).

FIG. 11 is a circuit configuration of an embodiment of the write data control circuit 40 shown in FIG. 3. The write data control circuit 40 includes inverters I64~I72, and CMOS transfer gates C16~C19.

FIG. 11 shows a circuit for outputting through the data input/output lines ((I/O11~1k)1~4) the data input through the data input/output lines (I/O11~1k). A circuit (not shown) for outputting the data input from the data input/output lines ((I/O21~2k)1~4)~((I/On1~nk)1~4) to the data input/output lines ((I/O21~2k)1~4)~((I/On1~nk)1~4) is of the same configuration as that of FIG. 11.

Next, the operation for the elements shown in FIG. 11 will be explained.

The CMOS transfer gates C16~C19 respectively transfer the data input from the data input/output lines (I/O11~1k) in response to the write control signal PWCMD of high level. The inverters (I65, I66), (I67, I68), (I69, I70), and (I71, I72) respectively perform a buffering operation for the data output from the CMOS transfer gates C16~C19 and then output the buffered data to the data input/output lines ((I/O11~1k)1~4).

US 6,888,366 B2

11

In other words, the write data control circuit 40 shown in FIG. 11 simultaneously outputs the data input from the data input/output lines (I/O11~1k) in response to the write control signal PWCMD to the data input/output lines ((I/O11~1k)1~4)).

As described above, the control circuit according to an embodiment of the present invention uses the latch timing control signal PRCMD2 for correctly latching the data, but may be constituted of latching the data with read control signals without using the latch timing control signal PRCMD2.

Further, the control circuit of the present invention may be incorporated in the probe card, and may be also incorporated separately between the tester and the probe card.

Accordingly, the semiconductor chip test system and test method thereof can simultaneously test many semiconductor chips regardless of the number of data input/output pads(or, pins).

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A semiconductor chip test system, comprising:

a tester having a plurality of data input/output pins for inputting/outputting data through the plurality of data input/output pins;

a plurality of semiconductor chips to be tested by the tester; and

a control circuit for sequentially outputting the data output from each of the plurality of semiconductor chips to the tester during a read operation and supplying the data input from the tester to the plurality of semiconductor chips during a write operation, wherein the control circuit, comprises:

a clock signal generating means for generating a first clock signal in response to a rising edge of a clock signal input from the tester and generating a second clock signal in response to a falling edge of the clock signal input from the tester;

a control signal generating means for generating a read command and a write command by inputting a command input from the tester;

a read control signal generating means for sequentially generating a plurality of a read control signals in response to the read command and the second clock signal;

a write control signal generating means for generating a write control signal in response to the write command;

a read data control means for sequentially outputting the output data from each of the plurality of semiconductor chips in response to the plurality of read control signals to the tester; and

a write data control means for simultaneously outputting the data input from the tester to the plurality of semiconductor chips in response to the write control signal.

2. A semiconductor chip test system, comprising:

a tester having n groups of data input/output pins of which each of the groups include k data input/output pins for inputting/outputting data through the plurality of data input/output pins;

n groups of semiconductor chips, each group including m semiconductor chips, each semiconductor chip com-

12

prising k data input/output pads (or pins) to be tested by the tester; and

a control means for sequentially outputting the data input from a first one to m_{th} one of each of the n groups of semiconductor chips to the tester during a read operation and simultaneously supplying nk data output from the tester to the n groups of semiconductor chips during a write operation, wherein the control means, comprises:

a clock signal generating means for generating a first clock signal in response to a rising edge of a clock signal input from the tester and generating a second clock signal in response to a falling edge of the clock signal input from the tester;

a control signal generating means for generating a read command and a write command by inputting a command input from the tester;

a read control signal generating means for sequentially generating m read control signals by inputting the read command in response to the second clock signal;

a write control signal generating means for generating a write control signal in response to the write command;

a read data control means for sequentially outputting the output data from a first semiconductor chip to the m_{th} semiconductor chip of each of the n groups of semiconductor chips to the tester in response to the m read control signals; and

a write data control means for simultaneously outputting the data input from the tester to the n groups of semiconductor chips in response to the write control signal.

3. The semiconductor chip test system according to claim 2, wherein the control signal generating means, comprises:

a read command generating circuit for generating the read command in response to the first clock signal, when an inverted low address strobe signal of high level, an inverted write enable signal of high level, and an inverted column address strobe signal of low level are supplied to the control signal generating means; and

a write command generating circuit for generating the write command in response to the first clock signal, when the inverted low address strobe signal of high level, the inverted column address strobe signal of low level, and the inverted write enable signal of low level are supplied to the control signal generating means.

4. The semiconductor chip test system according to claim 3, wherein the control signal generating means further comprises:

a precharge command generating circuit for generating a precharge command in response to the first clock signal, when the inverted low address strobe signal of low level, the inverted write enable signal of low level, and the inverted column address strobe signal of high level are supplied to the control signal generating means.

5. The semiconductor chip test system according to claim 2, wherein the read control signal generating means, comprises:

a read control signal generating circuit for sequentially generating a first read control signal in response to the second clock signal, when the read command is generated, and sequentially generating 2_{nd}~m_{th} read control signals by sequentially delaying the first read control signal by one clock cycle, in response to the second clock signal, when the first read control signal is generated; and

US 6,888,366 B2

13

a latch timing control signal generating circuit for generating a latch timing control signal by inputting the read control signal and the first clock signal.

6. The semiconductor chip test system according to claim 5, wherein the read data control means, comprises:

a first read data generating circuit for outputting the output data from a first semiconductor chip for each of the n groups of semiconductor chips to the tester; and

a second read data generating circuit for latching the output data from a second semiconductor chip of each of the n groups of semiconductor chips in response to the latch timing control signal, and sequentially outputting the output data from the second semiconductor chip to the m_{th} semiconductor chip of each of the n groups of semiconductor chips in response to each of the $2_{nd} \sim m_{th}$ read control signals to the tester.

7. The semiconductor chip test system according to claim 2, wherein the write control signal generating means generates the write control signal according to the generation of the write command, and disables the write control signal according to the generation of the read command or the precharge command.

8. A semiconductor test method for a semiconductor chip test system, the system including a tester having n groups of data input/output pins of which each of the groups include k data input/output pins for inputting/outputting data through the data input/output pins; and

n groups of semiconductor chips being respectively including m semiconductor chips, and each of the m semiconductor chips comprising k data input/output pads (or pins) to be tested by the tester, comprising steps of:

sequentially outputting the input data from a first semiconductor chip to m_{th} semiconductor chip for each of the n groups of the semiconductor chips to the tester during a read operation; and

simultaneously supplying nk data output from the tester to the n groups of semiconductor chips during a write operation, wherein the test method further comprises

generating a first clock signal in response to a rising edge of a clock signal input from the tester, generating a second clock signal in response to a falling edge of the clock signal from the tester, and generating a read command and a write command by inputting a command input from the tester;

generating sequentially m read control signals by inputting the read command in response to the second clock signal, and generating a write control signal in response to the write command; and

14

outputting sequentially output data from the first semiconductor chip to the m_{th} semiconductor chip for each of the n groups of semiconductor chips to the tester in response to each of the m read control signals during the read operation and simultaneously outputting the data input from the tester to the n groups of semiconductor chips in response to the write control signal during the write operation.

9. The semiconductor test method according to claim 8, wherein the step for generating the read command and write command comprises steps of:

generating the write command in response to the first clock signal, when the inverted low address strobe signal of high level, the inverted column address strobe signal of low level, and the inverted write enable signal of low level are supplied from the tester; and

generating the read command in response to the first clock signal, when the inverted low address strobe signal of high level, the inverted column address strobe signal of low level, and the inverted write enable signal of high level are supplied from the tester.

10. The semiconductor test method according to claim 8, wherein the step for generating the read and write control signals comprises steps of:

generating a first read control signal in response to the second clock signal, when the read command is generated, sequentially generating $2_{nd} \sim m_{th}$ read control signals that are delayed by one clock cycle from the first read control signal in response to the second clock signal, when the first read control signal is generated, and generating the latch timing control signal by inputting the read control signal and the first clock signal; and

generating the write control signal in accordance with generation of the write command, and disabling the write control signal in accordance with generation of the read command or the precharge command.

11. The semiconductor test method according to claim 8, wherein the step for controlling the read data, comprises:

outputting the output data from a first semiconductor chip for each of n groups of semiconductor chips to the tester in response to the first read control signal; and

latching the output data from a second semiconductor chip for each of n groups of semiconductor chips in response to the latch timing control signal, and sequentially outputting the output data from the second semiconductor chip to the m_{th} semiconductor chip for each of the n groups of semiconductor chips in response to each of the $2_{nd} \sim m_{th}$ read control signals to the tester.

* * * * *